PAS202BC SINGLE-CHIP CMOS VGA COLOR DIGITAL IMAGE SENSOR
PAS202BB SINGLE-CHIP CMOS VGA B&W DIGITAL IMAGE SENSOR

General Description

The PAS202B is a highly integrated CMOS active-pixel image sensor that has a VGA resolution of 644H x 484V. To have an excellent image quality, the PAS202B outputs 10-bit RGB raw data through a parallel data bus. It is available in color or monochrome and in 28-pin LCC.

The PAS202B can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register sets, it performs on-chip frame rate adjustment, offset correction DAC, programmable gain control, 10-bits ADC and 8-bits output formatting.

Features

- **VGA(644 x 484 pixels) resolution, ~1/4" Lens**
- **Bayer-RGB color filter array**
- **On-chip 10-bit pipelined A/D converter**
- **User selectable digital output formats:**
  - **10-bit parallel RGB raw data**
  - **10/8-bit formatted data**
- **On-chip 9-bit background compensation DAC**
- **On-chip programmable gain amplifier**
  - **4-bit color gain amplifier(x3)**
  - **5-bit global gain amplifier (x5)**
- **Continuous variable frame time(1/2sec~1/30sec)**
- **Continuous variable exposure time**
- **I2C Interface**
- **Digitally programmable registers**
- **Single 3.3V supply voltage**
- **100 mW low power dissipation**
- **350 uW low power down dissipation**
- **Flash light timing**
- **Mirror output**

Key Specification

Supply Voltage	3.3V ± 10%
Resolution	644(H) x 484(V)
Array diagonal	4.5mm (~1/4"Optic)
Pixel Size	5.6μmX5.6μm
Frame rate	~30 fps
System clock	Up to 48 MHz
Max. pixel rate	12MHz
FPN	TBD
Sensitivity	1.5V/Lux-sec(green)
PGA gain	29.5 dB max.
Color filter	RGB Bayer Pattern
Exposure Time	~ Frame time to 4 pxclk
Scan Mode	Progressive
S/N Ratio	>42 dB
Package	28 pins LCC

PixArt Imaging Inc.
E-mail: fae_service@pixart.com.tw

1. Pin Assignment

PIN No.	PIN NAME	Type	Definition
1	VSSAY	GND	Analog ground
2	VLRST	BIAS	Fixed bias input voltage, 1.65V
3	PXD<9>	OUT	Digital data output
4	PXD<8>	OUT	Digital data output
5	PXD<7>	OUT	Digital data output
6	PXD<6>	OUT	Digital data output
7	PXD<5>	OUT	Digital data output
8	VDDQ	PWR	Digital VDD, 3.3V
9	VSSQ	GND	Digital ground
10	PXD<4>	OUT	Digital data output
11	PXD<3>	OUT	Digital data output
12	PXD<2>	OUT	Digital data output
13	PXD<1>	OUT	Digital data output
14	PXD<0>	OUT	Digital data output
15	SYSCLK	IN	Master clock input
16	PXCLK	OUT	Pixel clock output
17	HSYNC	OUT	Horizontal Synchronization clock
18	VSYNC	OUT	Vertical Synchronization clock
19	SCL	IN	I2C clock
20	SDA	I/O	I2C bi-directional data
21	VDDD	PWR	Digital VDD, 3.3V
22	VSSD	GND	Digital ground
23	CSB	IN	Chip select
24	VCM	BYPASS	Analog voltage reference
25	VRT	BYPASS	Analog voltage reference
26	VRB	BYPASS	Analog voltage reference
27	VSSA	GND	Analog ground
28	VDDA	PWR	Analog VDD, 3.3V

2. Block Diagram

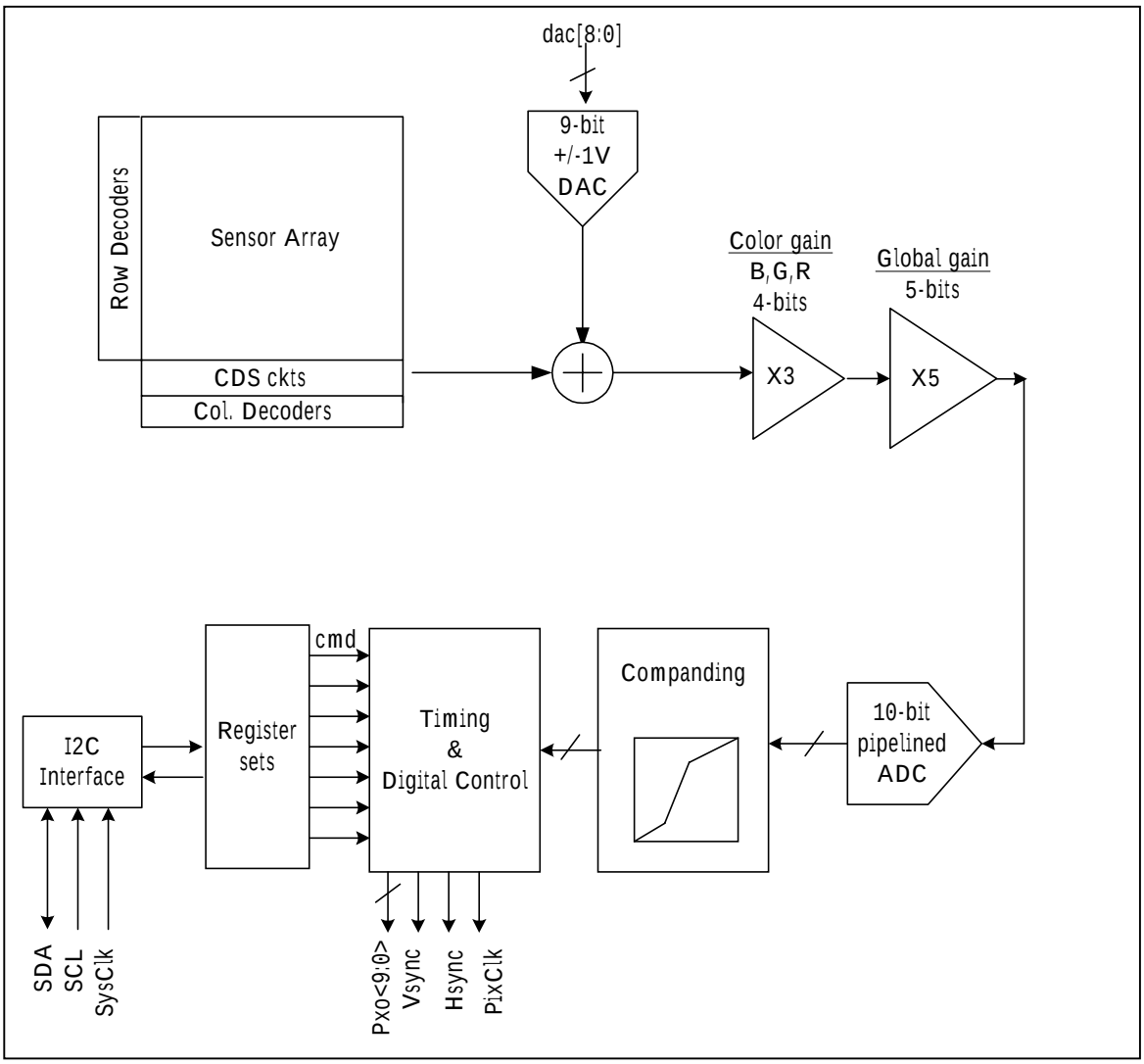


Fig 2.1 – Block diagram of the PAS202B

3. Register and operation

3.1. Resister list

Slave ID = 1000,000,R/W
Part ID = 0000,0001,0111
Ver ID = 0000

Register	Name	R/W	Default	Description
Reg_0 [7:0]	PartID[11:4]	R	00000001	Part ID
Reg_1 [7:4]	PartID[3:0]	R	0111	Part ID
Reg_1 [3:0]	VerID[3:0]	R	0	Version ID
Reg_2 [7:6]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_2 [5:0]	Np[5:0]	R/W	000100	Np=system clock/pixel clock
Reg_3 [7:0]	Nov_by2[7:0]	R/W	01011001	Sync width =(2* Nov_by2–8)pixclk [120(min)pxclk ~ 504 (max) pxclk]
Reg_4 [7:0]	lpf[13:6]	R/W	00000111	Line per frame
Reg_5 [7:6]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_5 [5:0]	lpf[5:0]	R/W	100101	Lpf=485d~16383d
Reg_6 [7:4]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_6 [3:0]	cgn_dk[3:0]	R/W	0	color gain for dark pixel
Reg_7 [7:4]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_7 [3:0]	cgn_B[3:0]	R/W	0	color gain for blue pixel
Reg_8 [7:4]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_8 [3:0]	cgn_G[3:0]	R/W	0	color gain for green pixel
Reg_9 [7:4]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_9 [3:0]	cgn_R[3:0]	R/W	0	color gain for red pixel
Reg_10[7:0]	RSV	R/W	0	Reserved.
Reg_11[7:6]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_11[1]	dac[8]	R/W	0	sign bit for DAC, (default 0:positive)
Reg_12[7:0]	dac[7:0]	R/W	0	Magnitude for DAC
Reg_13[7:0]	RSV	R/W	0	Reserved(Please set as “00001100”.)
Reg_14[7:1]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_14[0]	offset_ny[0]	R/W	0	exposure time: line offset (Please set offset_ny >0)
Reg_15[7:0]	offset_ny[8:1]	R/W	0	
Reg_16[7:5]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_16[4:0]	global[4:0]	R/W	0	PGA global gain
Reg_17[7:1]	RSV	R/W	0	Reserved(Please set as “0”.)
Reg_17[0]	i2c_update_sync_flag	R/W	0	i2c_update_sync_flag
Reg_18[7:3]	RSV	R/W	0	Reserved(Please set as “0”)
Reg_18[2:0]	Formatting[2:0]	R/W	0	Data formatting (Please set as “101”.)
Reg_19[7:0]	RSV	R/W	0	Reserved (Please set as “01100011”.)
Reg_20[7:0]	RSV	R/W	0	Reserved
Reg_21[7:0]	RSV	R/W	0	Reserved (Please set as “01110000”.)
Reg_22[7:0]	RSV	R/W	0	Reserved
Reg_23[7:0]	RSV	R/W	0	Reserved
Reg_24[5:0]	RSV	R/W	0	Reserved

3.2. Exposure Time calculation and programming example

The Exposure Time calculation of PAS202B is based on the following sequence:

1. System clock
2. Pixel clock
3. Frame rate
4. Exposure time
5. Equivalent exposure line and pixel number
6. Register offset_ny

For a given system clock, pixel clock and fps (frame per second):

Np = system clock / pixel colck

lpf = Int [pixel clock / (772*fps)].

Exposure time can be expressed as pxclk count of "**pxclk/120"** as long as exposure time is multiple of "1/120" seconds. Note that:

- 100,000 pxclk @12Mhz, exposure time = 1/120 second.
- 200,000 pxclk @12Mhz, exposure time = 2/120 second.
- 300,000 pxclk @12Mhz, exposure time = 3/120 second.

Programming example:

Example 1:

Given system clock: 48MHz

Pixel colck: 12MHz

exposure time: 3/120 sec

lpf: 485

Then, **Np** = system clock / pixel clock = 48 /12 = 4

exposure pxclk = exposure time * pixel clock = (3/120)*12M = 300,000 pxclk

exposure line = Int[exposure pxclk/772] line = 388 lines

offset_ny = (lpf+1)-exposure time = 486 - 388 = 98

Example 2:

Given system clock: 48MHz

Pixel clock: 12MHz

exposure time 4/120 sec

lpf = 527 (i.e fps=29.49)

Then, **Np** = system clock / pixel clock = 48 /12 = 4

exposure pxclk = exposure time * pixel clock = (4/120)*12M = 400,000 pxclk

exposure time = Int[exposure pxclk/772] lines

= 518lines

offset_ny = (lpf+1)-exposure time **= 528 - 518 =10**

4. Output Format

4.1. Pixel Array And Pixel Color Pattern

The output image format of PAS202B is VGA (640x480 pixel array). To provide the co-processor with the extra information it needs for interpolation at the edges of the pixel array, an border of 2 pixels on all 4 sides of the array are available. Fig 4.1. illustrates the pixel array and pixel color pattern.

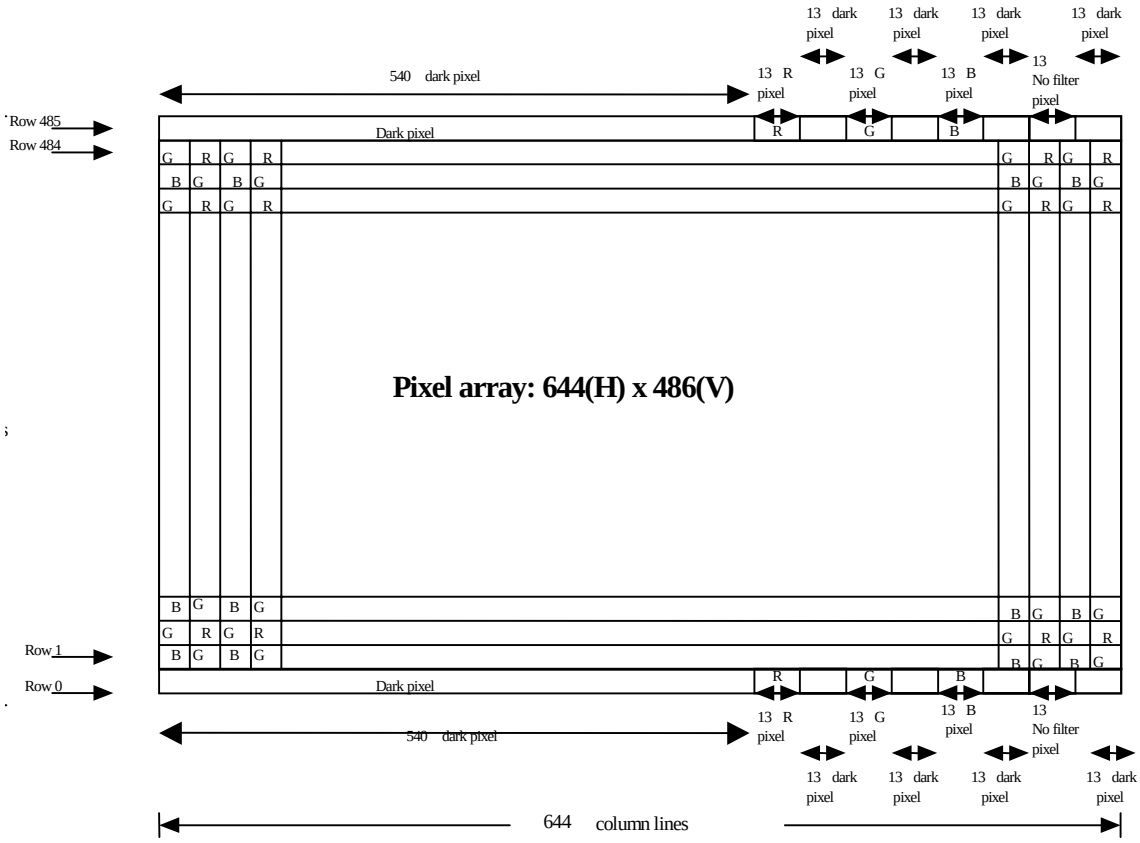


Fig 4.1. Pixel array and pixel color pattern

Note:

1. Pixel color pattern does not apply to monochrome sensor.
2. Pixel read-out proceeds from left to right, and from bottom row to top row.
3. Pixel array not drawn to scale.

4.2 Output timing:

4.2.1. Normal readout:

Pixel per line is programmable, 772 pixels ~ 1156 pixels.

4+4 blank pixel for each line. (See Fig 4.2. Fig 4.3)

1+1 Dark line for each frame.(See Fig 4.4. Fig 4.5)

Dark line output format: Fig 4.6.

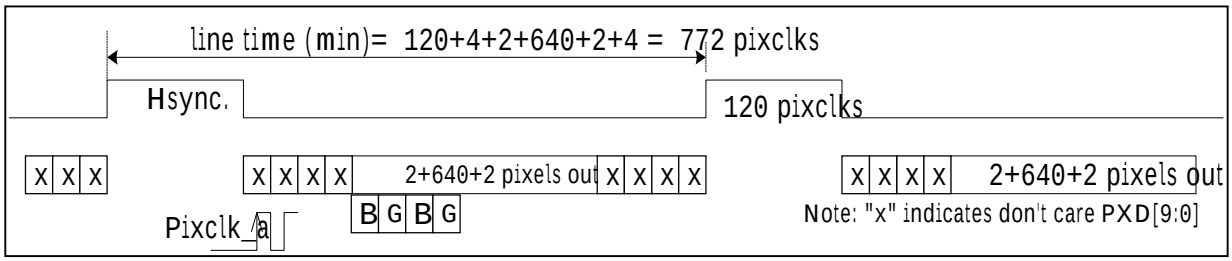


Fig 4.2. Inter-line timing (default)

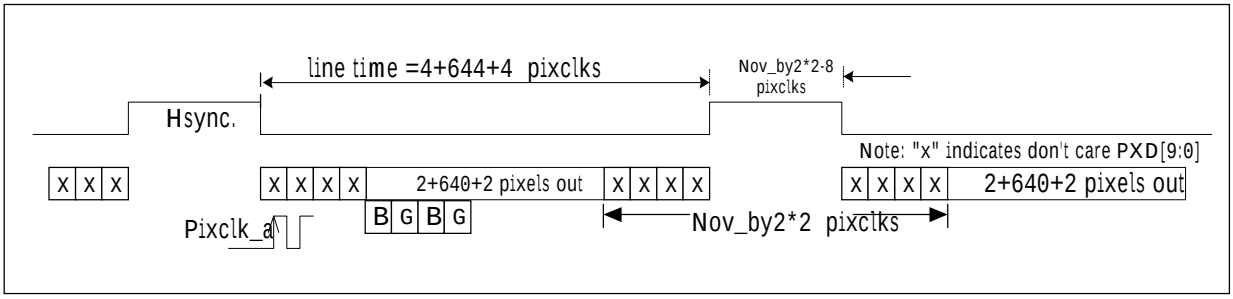


Fig 4.3. Inter-line timing (programmable)

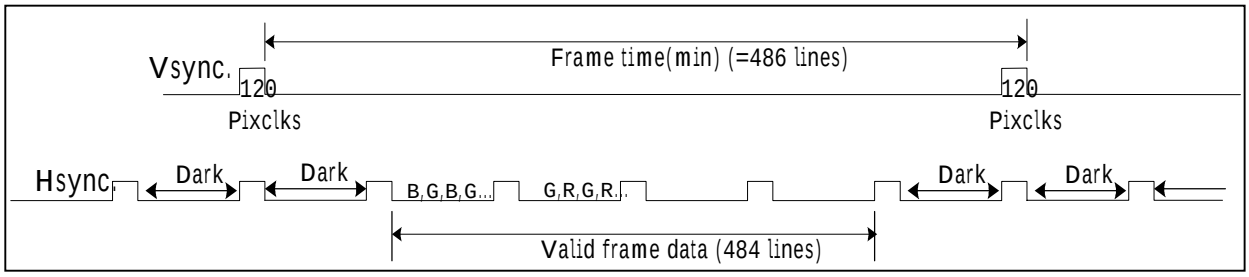


Fig 4.4. Inter-frame timing (default)

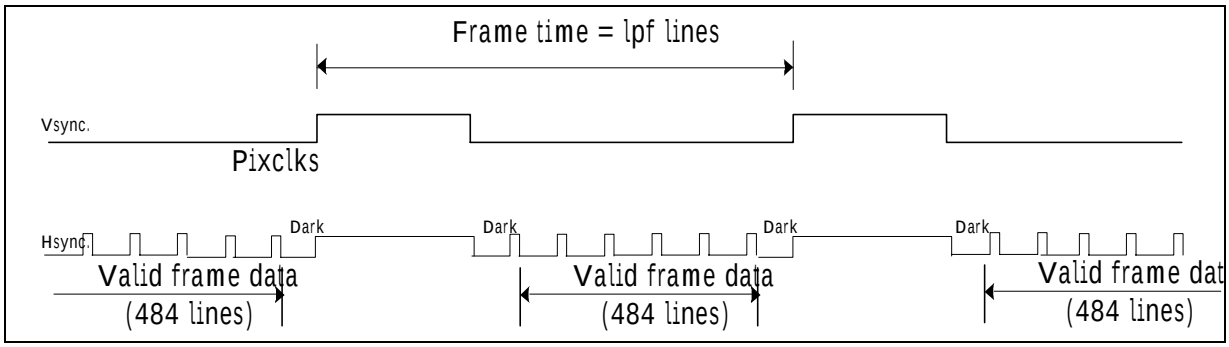


Fig 4.5. Inter-frame timing (programmable)

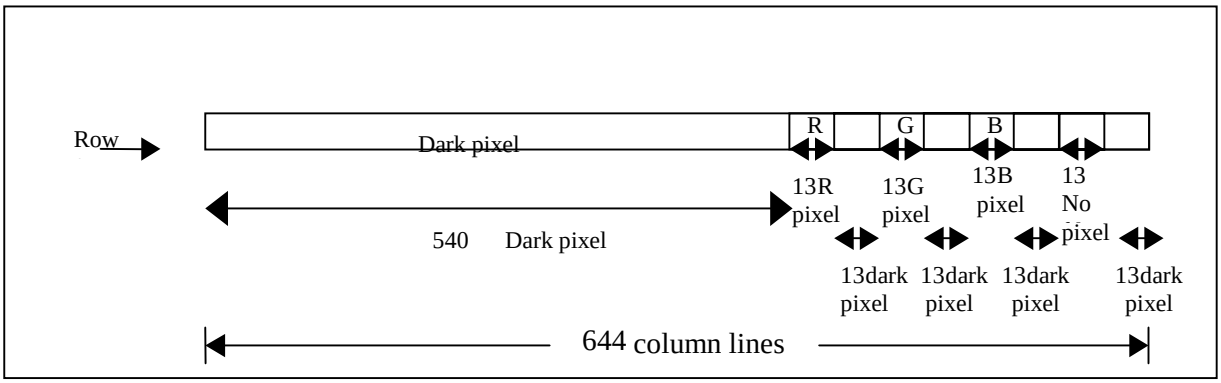


Fig 4.6. Dark line output format

4.3 Data Formatting

The PAS202B provides the formatting function which allows coding of the output bits to perform on-chip contrast adjustments. The user can select one of the 5 transformation ing curves shown in Fig 4.7. by setting the Reg_18 as follows:

Default: 'b xxxxx0xx (without formatting, 10bit data output)

Curve 0: 'b xxxxx100

Curve 1: 'b xxxxx101

Curve 2: 'b xxxxx110

Curve 3: 'b xxxxx111

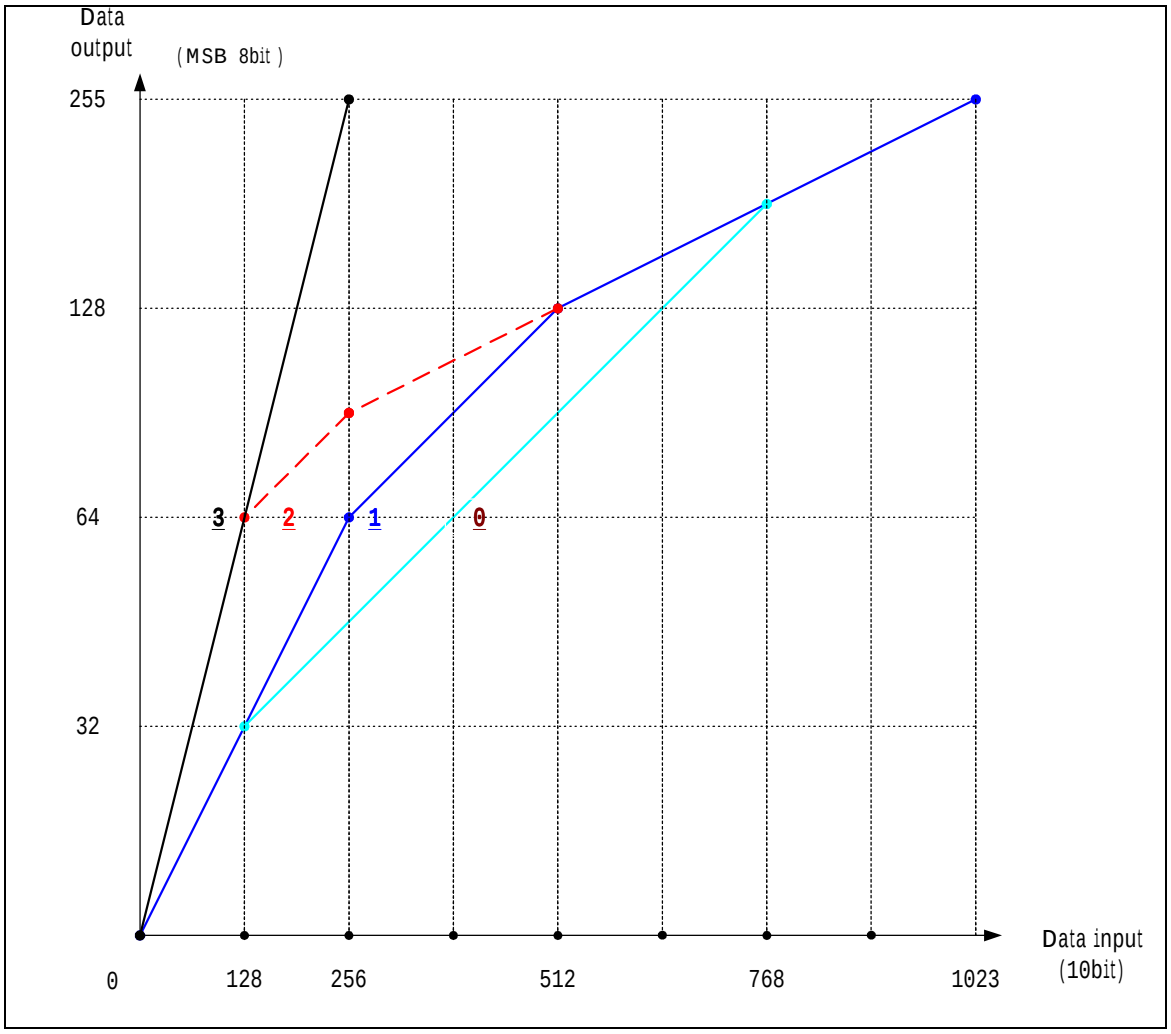


Fig 4.7. Available formatting curves

5. Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vdd	DC supply voltage	-0.5	3.8	V
Vin	DC input voltage	0.5	Vdd+0.5	V
Vout	DC output voltage	-0.5	Vdd+0.5	V

DC Electrical Characteristics (VDD=3.3V±10%, Ta=0°C~40°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type :PWR					
VDD	Analog and digital operating voltage	3.00	3.3	3.60	V
IDD	Operating Current		30		mA
Type :IN & I/O Reset and SYSCLK					
VIH	Input voltage HIGH	2.0		VDD	V
VIL	Input voltage LOW	0		0.8	V
Cin	Input capacitor			10	pF
Ilkg	Input leakage current			1.0	uA
Type : OUT & I/O for PXD0:9, PXCLK, H/VSYNC & SDA, load 20pf, 3.3volts					
VOH	Output voltage HIGH	Vdd-0.2			V
VOL	Output voltage LOW			0.2	V

AC Operating Condition

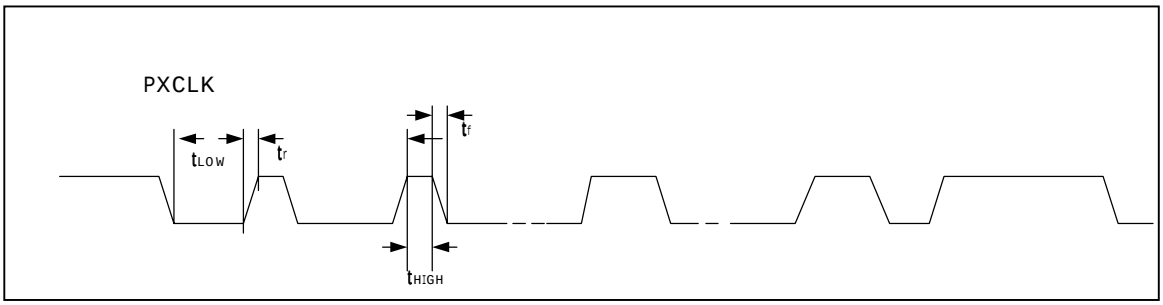
Symbol	Parameter	Min.	Typ.	Max.	Unit
fsysclk	Master clock frequency	8		48	MHz
fpxclk	Pixel clock output frequency			12	MHz

Sensor Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Photo response non-uniformity	PRNU		1.7		%	
Saturation output voltage	Vsat.		1.2		V	
Dark output voltage	Vdark		TBD		Lsb/sec	
Dark signal non-uniformity	DSNU		2.79		Lsb	
Sensitivity (Red channel)	R		1.9		V/Lux-sec	
Sensitivity (Green channel)	G		1.5		V/Lux-sec	
Sensitivity (Blue channel)	B		1.1		V/Lux-sec	
Column non-uniformity	Cnu			1.56	%	

PXCLK Timing Specification @12M Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{LOW}	Low period of the PXCLK duty cycle	40%	50%	60%	%
t_{HIGH}	High period of the PXCLK duty cycle	40%	50%	60%	%
t_r	Rise time signal		10		ns
t_f	Fall time signal		10		ns
C_b	Capacitive load for each bus line		15		pF



6. Package Information

6.1. Pin Connection Diagram

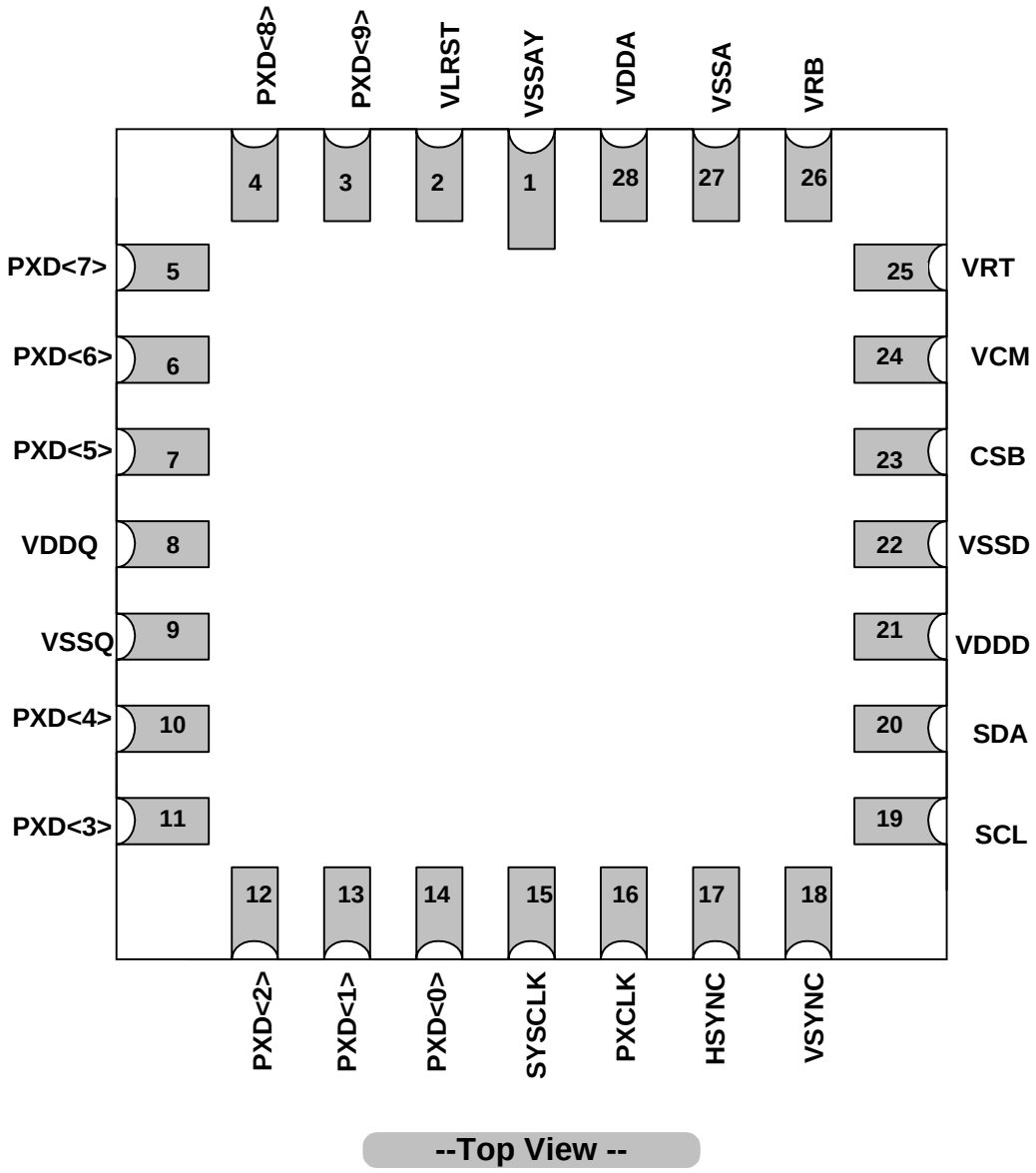
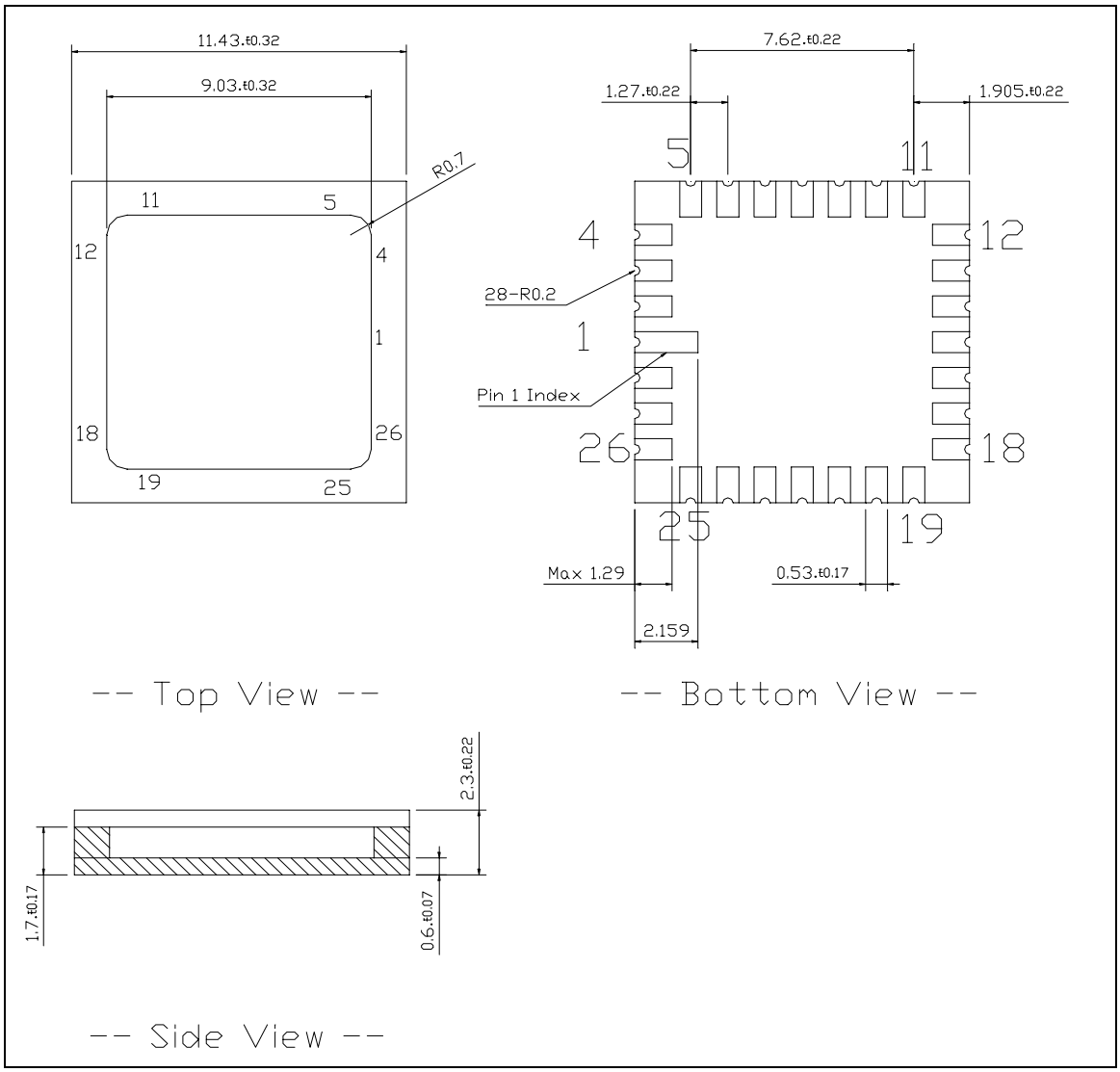
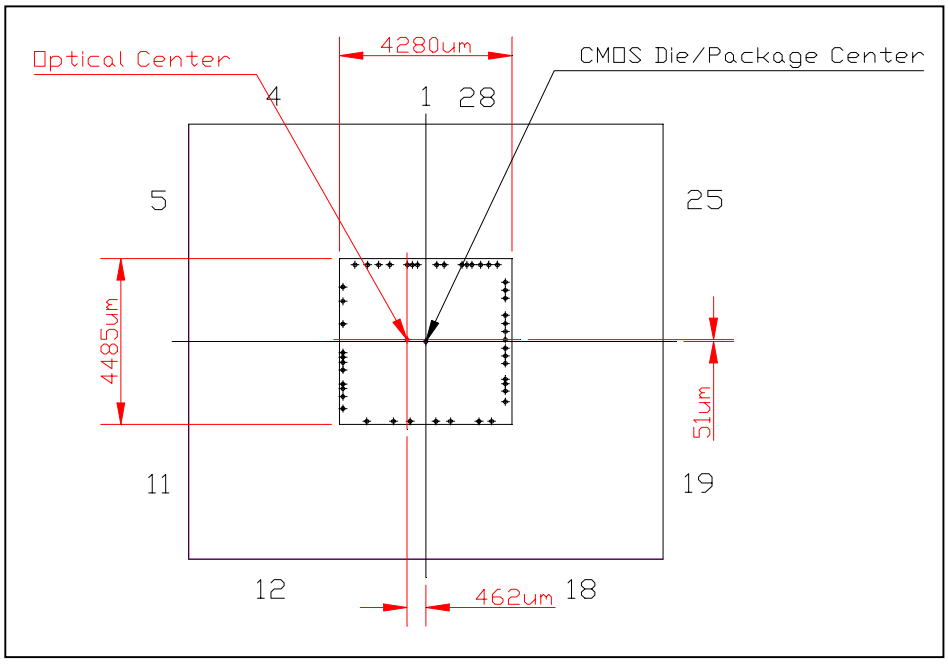


Fig. 6.1. Pin connection of PAS202B in 28 LCC package

6.2. Package Outline



6.3. Optical Center(Sensor Array Center)and Die/Package Center Offset



Note:

1. Die center = Package center
2. Chip offset tolerance : +/- 200um

7. Referencing Application Circuit