# ZMI 2002
# Measurement Board
## P/N 8020-0211-01
# Operation Manual
# OMP-0413G



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## MANUAL REVISION INFORMATION

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| D | June 1998 | | |
| E | November 1998 | | |

## MANUAL NOTATIONS

**Warning!** Denotes a hazard that could cause injury to personnel, and can also cause damage to the equipment.

**Note:** Provides helpful information.

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d. Requires replacement because of decomposition due to chemical action.
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01/96

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# *Chapter 1* Introduction

### *In This Chapter*


1-1 Background

1-2 ZMI-2002 Measurement Board
- VMEbus Interface
- P2 Interface
- On-board Fiber Optic Detector
- Compatibility

1-3 Specifications


## 1-1 Background

The Zygo ZMI-2002 Measurement Board is a register based VMEbus circuit board. This manual makes the assumption that you are familiar with the VMEbus specification and interferometry principles.

> **Note:** Throughout this manual, a 0x in front of a number indicates that the number is hexadecimal, and an * (asterisk) used after a signal name indicates a negative true signal.

The VMEbus specification is described by ANSI/IEEE Standard 1014-1987, which is available from:

IEEE Customer Service
445 Hoes Lane, PO Box 1331
Piscataway, New Jersey, USA 08855-1331
phone: 800-678-4333 (in the United States and Canada)
908-981-0060 (outside the United States and Canada)
Internet: http://www.ieee.org

## 1-2 ZMI-2002 Measurement Board

This manual describes the installation and use of the ZMI-2002 Measurement Board. The Measurement Board is a component in a complete Zygo Motion Interferometer (ZMI) system. Figure 1-1 shows the basic structure of a ZMI system.

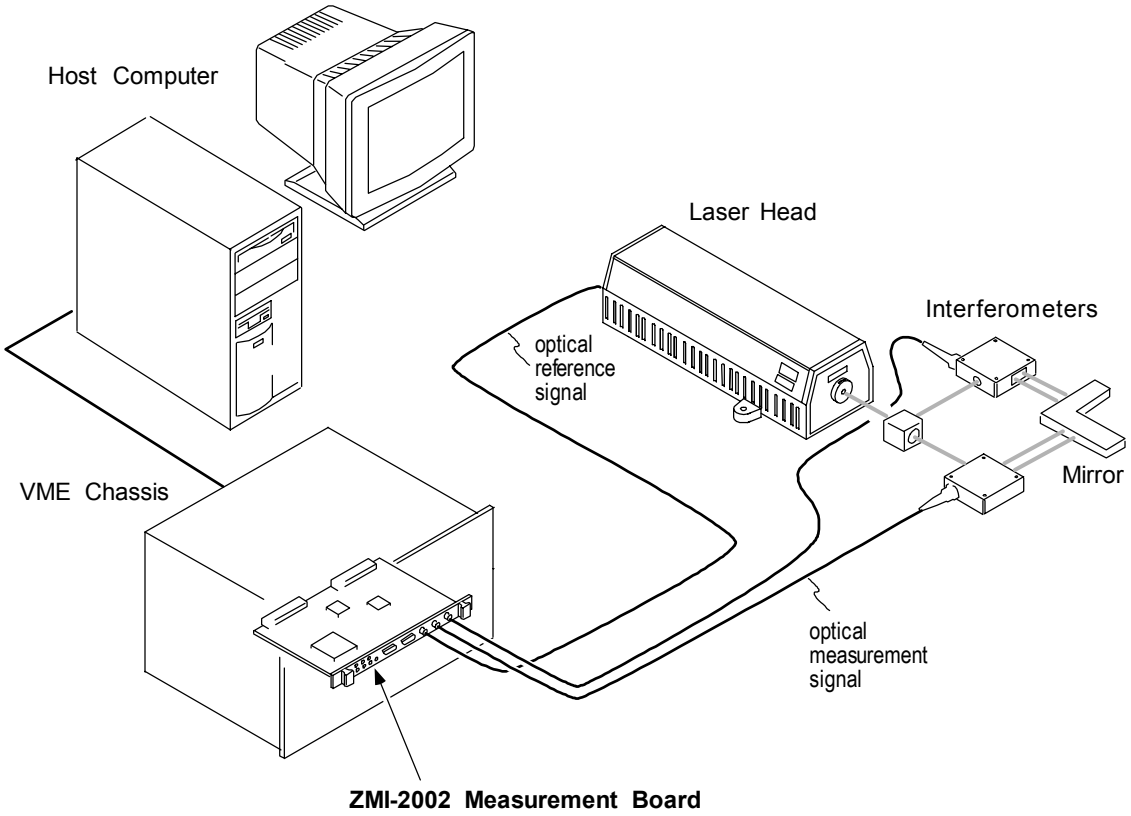



**Figure 1-1** Basic ZMI System

The Measurement Board is part of a total solution for an interferometry based motion measurement system. It can be used in Zygo's VME based interferometer system or incorporated into your own VME based system. Minimally, a displacement measuring interferometer system consists of a laser head, optics, and a Measurement Board.

The function of the Measurement Board is to convert a measurement signal from an interferometer and a reference signal from the laser head into measurement data in the form of a 36-bit (or 32-bit) 2's complement word.

The ZMI-2002 Measurement Board, shown in Figure 1-2, is a two axis, register based VME slave card used with Zygo motion measuring interferometers. Its circuitry converts the interference signal from one or two interferometers to position and velocity data. The Measurement Board complies electrically and mechanically with Revision C.1 (1987) of the VMEbus specification.

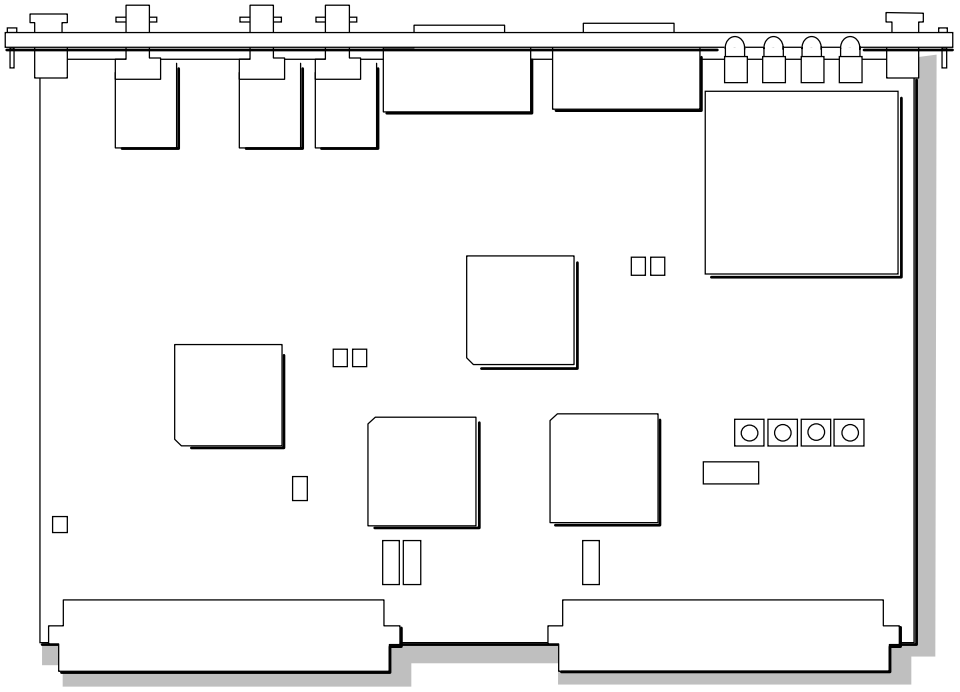


**Figure 1-2** ZMI-2002 Measurement Board

The ZMI-2002 Measurement Board has two independent data transfer options. Measurement data, including position, velocity, and time data, as well as system status information can be read through the VMEbus or the P2 interface. The user will need to program parameters internal to the ZMI system by writing through the VMEbus interface.

The following sections describe these interface options.

## *VMEbus Interface*

The ZMI-2000 VMEbus interface provides an efficient means to acquire motion data and system status from the ZMI system to a user program running on a VMEbus computer.

The VMEbus interface includes the following functions:

- Sampling of position, velocity, time, and error/status data.
- Digital filter coefficient programming.
- Offset register, user velocity limit, sample timer register.
- Programmable Interrupts.
- Optical power, calibration data for optical power and data age compensation.

These data and functions are located in discrete registers within the VMEbus address space. Each measurement axis in a ZMI system must be programmed to a unique base address. All motion data can be acquired through a VME read access of the appropriate offset from the board base address. The ZMI accumulates and latches motion data asynchronously to the VMEbus and is not affected by bus reads and writes.

The Zygo VME interface provides capability to transfer data using 16-bit or 32-bit word lengths. Typically all motion registers are 32 bits in length. However, the position data resides in 36-bit registers within the ZMI electronics. These registers can be accessed in three 16-bit transfers, or two 32-bit transfers, In addition, these registers can be configured to output any 32 bits of the 36 bits when the register is read.

VME functions include Status registers for indicating errors. Control registers are provided for setting modes of operation and for enabling interrupts. A Command register is provided for resetting error conditions and data accumulators.

The Measurement Board can generate VME interrupts on any one of the seven levels. All of the Measurement Board error conditions can be individually enabled to cause interrupts. The interrupt level is selected by a combination of a VME bus write accesses, storing an interrupt level code to an Interrupt Vector register and the placement of a hardware jumper on the board. Interrupts are enabled by various bits in the Interrupt Enable register. Interrupt jumper settings are shown in Chapter 2.

## *P2 Interface*

The P2 connector provides a secondary high speed interface for reading 36-bit (or 32-bit) position data, 32-bit time data, 32-bit velocity data, and error/status data. This interface has a separate addressing and bus control system permitting reading of data asynchronously from the VMEbus.

The P2 interface provides the following functions:

- External sampling or direct reading of position, velocity, time, and error/status data.
- Programmable, periodic automatic data sampling.
- Reset position accumulator.
- Reset time accumulator.
- Reset P2 interrupts.

## *On-board Fiber Optic Detectors*

The ZMI-2002 Measurement Board includes two on-board fiber optic detectors, shown in Figure 1-3. This feature eliminates the need for a separate receivers and reduces sensitivity to electrostatic discharge. The Measurement Board on-board detectors connect directly to a fiber optic cable, from either a fiber optic interferometer or a nonfiber optic interferometer with a fiber optic pickup. In both cases, the fiber optic cable directs the light from the interferometer to a photo detector on the Measurement Board.

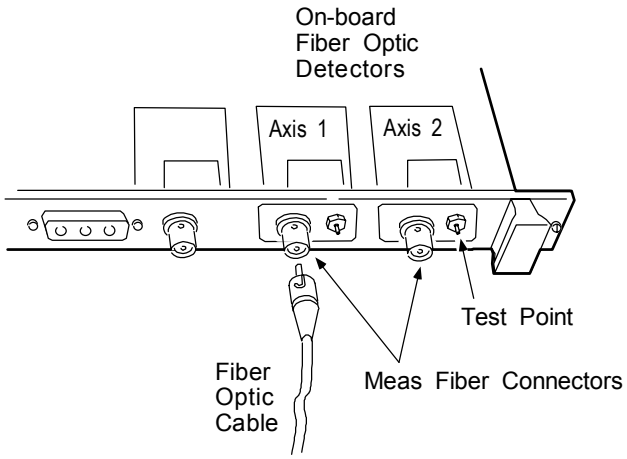



**Figure 1-3** On-board Fiber Optic Detectors

An analog test point is used when aligning the interferometer to ensure the best possible alignment. The interferometer alignment is adjusted to maximize the output voltage at the test point. The higher the voltage the greater the detected signal intensity. The specific output voltage varies depending upon the interferometer efficiency, the optical alignment, and other system tolerances. The minimum optical signal must be 5 microwatts, as measured at the entrance of a fiber optic pickup.

As an added convenience, the voltage level can be read through a register on the VMEbus.

### *Compatibility*

The Measurement Board is compatible with the following components: Zygo 7702 Laser Heads, fiber-optic pickup, and fiber-optic cables; and all industry standard interferometers and optics.

The Measurement Board is **not** compatible with the following Zygo components: the Zygo 2/20 electronics system, the 764Z Pulse Converter board, the ZMI-1000A Measurement Board, the 7081 Receiver, and the 7701 and 7701A Laser Heads.

The Measurement Board is not compatible with any Hewlett-Packard DMI electronic systems, but can be used with HP optical components.

## 1-3 Specifications

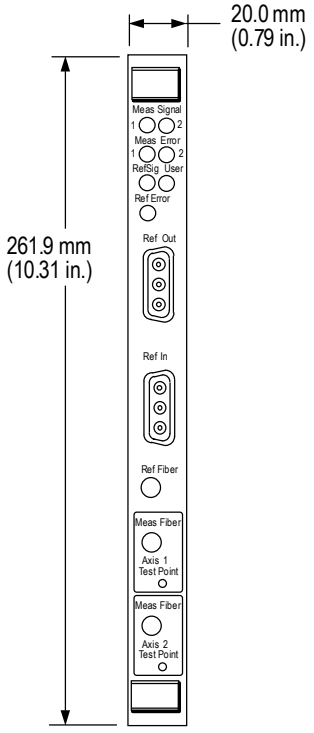
The general specifications of the ZMI-2002 Measurement Board are shown on the following page.

## ZMI-2002 Measurement Board
## P/N 8020-0211-01

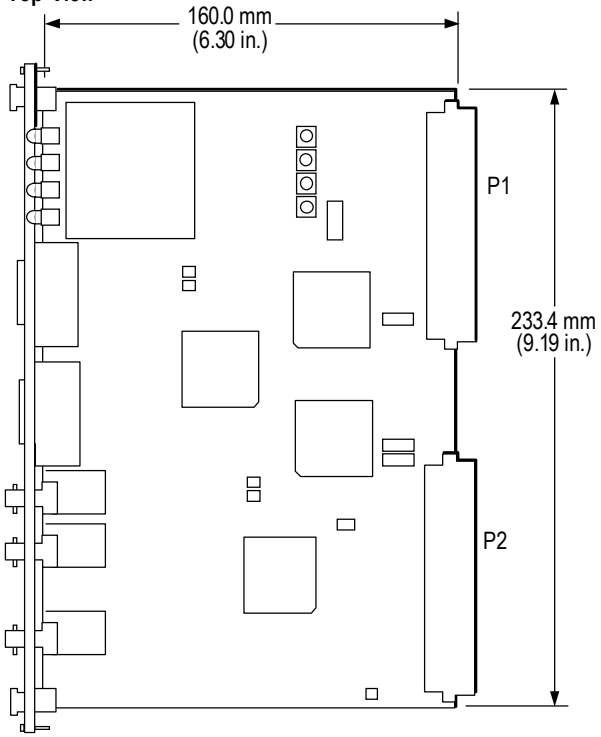
**Size:** See below.
**Number of Axes per Board:** 2
**Position Resolution:** λ/2048 (0.3 nm)
(double pass)
**Position Range:** ± 10.6 m @ λ/2048
**Position Format:** 36 bit - 2's complement
**Time Resolution:** 25 nanoseconds
**Time Range:** 107.4 seconds
**Time Format:** 32 bit - positive integer
**Velocity Resolution:**
dependent on digital filter Kp and Kv settings
0.7543552 µm/sec (typical)
**Velocity Range:** ± 2.1 m/sec (double pass)
**Velocity Format:** 32 bit - 2's complement
**Maximum Acceleration:** 100 g
**Data Age:** 335 nanoseconds
**Data Age Uncertainty:** ± 1.2 nanoseconds,
up to 6 axes (compensated)

**Recommended Input Intensity for On-board Fiber Optic Detector:** ≥5 µW
**Power Requirement:** +5 VDC ±5% @ 5.0 A
**Electronic Accuracy:**
@ 100 mm/sec ≤1.2 LSB
@ 1000 mm/sec ≤1.4 LSB
@ 2100 mm/sec ≤1.6 LSB
**Compliance:** UL94V0, UL796
**VME Compliance:**
VMEbus Specification Rev. C.1
6U Size
A16 or A24 Addressing
D16 or D32 Data Transfer
D08 (O) Interrupt Acknowledge Cycle
**Cooling Requirements:**
60 linear fpm minimum for 0 to 40° C
250 linear fpm minimum for 0 to 55°C
**Operating Environment:**
Temperature: 0 to 55° C
Humidity: 0 to 90% (non-condensing)

**Front Panel**




**Top View**



# *Chapter 2* **Installation**

### *In This Chapter*


2-1 System Interconnections
2-2 Installing the Measurement Board in a VME Backplane
- Basic Requirements of the VME Chassis
- Noise and Interference

2-3 Installation Summary
- VMEbus Base Address Selection
- VME Interrupt Selection
- P2 Bus Base Address Selection
- Recommended Grounding

2-4 Switch and Jumper Summary
2-5 Front Panel Connectors
- Meas Fiber and Ref Fiber Connectors
- Connecting Fiber Optic Cables
- Ref In and Ref Out Connectors

2-6 Backplane Connectors
- P1 Connector and Pin Assignments
- P2 Connector and Pin Assignments
- P2 Signal Termination


## 2-1 System Interconnections

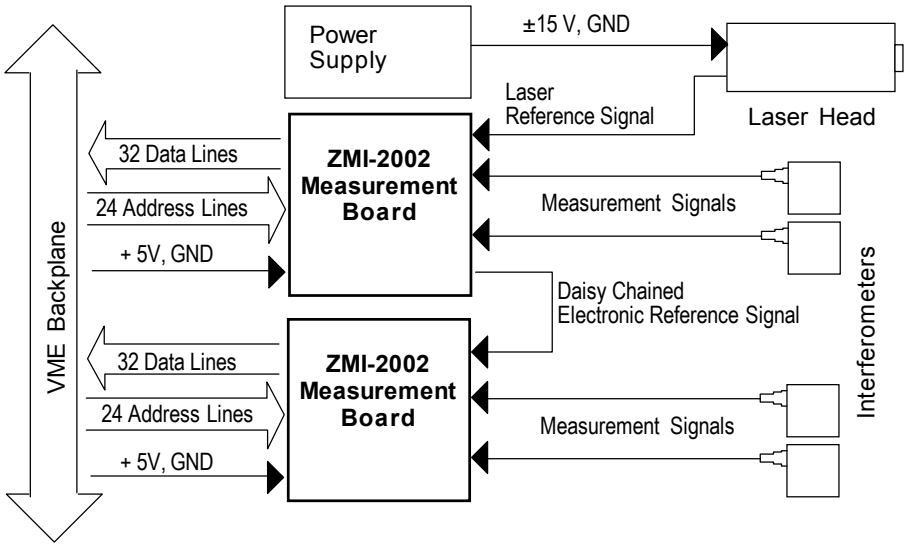



**Figure 2-1** System Interconnections

A general system configuration is shown in Figure 2-1. The laser head provides an optical reference signal to the first Measurement Board, which then provides a synchronized electronic reference signal to other Measurement Boards in the system. The optical measurement signals are provided directly from the interferometer through a fiber optic connection. The reference signal is also used to minimize data age uncertainty.

## 2-2 Installing the Measurement Board in A VME Backplane

### *Basic Requirements of the VME Backplane*

The Measurement Board may be installed in a user-supplied VME backplane. Ensure that the user VME backplane meets the following basic requirements:

- Supplies incoming DC voltage for the board: +5 VDC, ±5% @5.0A
- Provides a cooling air flow of at least 60 linear feet per minute for operation in a temperature range from 0 to 40 degrees Celsius, or at least 250 linear feet per minute for 0 to 55 degrees Celsius.
- Supplies a level of noise and interference immunity.

### *Noise and Interference*

Noise and interference caused by other system components, such as switching power supplies and fans, can degrade the accuracy of the Measurement Board. The possible symptoms are: apparent noise in the position data output, Meas Error LED on, or Ref Error LED on.

It is recommended to check performance when installing the Measurement Board in a user-supplied chassis. To perform the check, install the Measurement Board and the Laser Head, according to their installation instructions. As shown in Figure 2-2, position a fiber optic pickup directly in the Laser Head output beam with no interferometer. In this configuration, and after a system reset, the position data should be stable to ±1 LSB with no error LEDs on. If the data is not stable or there are error LEDs on, noise interference is indicated. Potential noise sources are listed in Table 2-1.

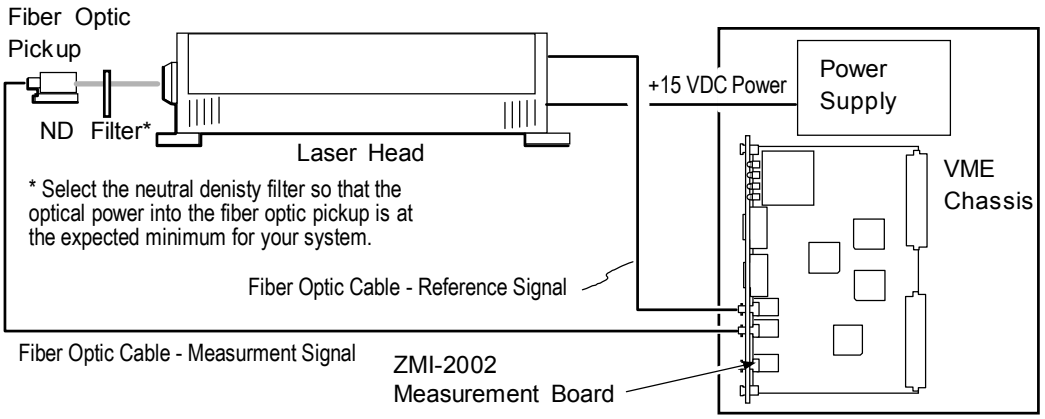



**Figure 2-2** Typical System Noise Test

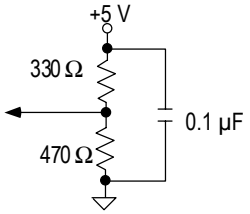
| *Noise/Interference Source* | *Guidelines* |
|---|---|
| Switching Power Supplies | Switching power supplies can cause transients on the power supply conductors at harmonics of the switching frequency. Follow the installation and noise suppression recommendations of your power supply manufacturer. |
| DC Brushless Fans | DC brushless fans can also cause transients on the power supply conductors. Follow the installation and noise suppression recommendations of your fan manufacturer. |
| VME Backplane | Use passive termination not active termination. The recommended termination circuit is shown here.   |
| Improper Component Grounding | Improper grounding of the Measurement Board, laser head, or cables, may cause measurement data noise. To eliminate this possibility, conform to the guidelines in the "Recommended Grounding" section in this chapter. |

**Table 2-1** Possible Noise Sources in User-supplied VME Chassis

## 2-3 Installation Summary

To install the Measurement Board in the VME chassis, proceed as follows. Refer to Figures 2-3 and 2-4. Greater detail on some of these steps are provided in the following sections. Section 2-4 provides a summary of the switch and jumper settings.

> ⚠ **Warning!**
> Use proper handling techniques when touching the Measurement Board to prevent the board from being damaged by electrostatic discharge (ESD). The board should be stored in a static shield bag and handled only by individuals using a static control wrist grounding strap.

1. Using a static control wrist strap, remove the board from the static shield bag.
2. Select A16 or A24 address mode with jumper JN5.
3. Select the VMEbus base address with switches SW3 and SW4 for A16 address mode or switches SW1, SW2, SW3, and SW4 for A24 address mode. Each board in the system must have a unique address setting.
4. Set jumper JN9 to the desired VME interrupt level for each board.
5. Set jumper JN5 for the desired reset mode. Jump pins 1-3 to reset board using VMEbus SYSRESET* signal; jump pins 3-5 for board reset at power-on.

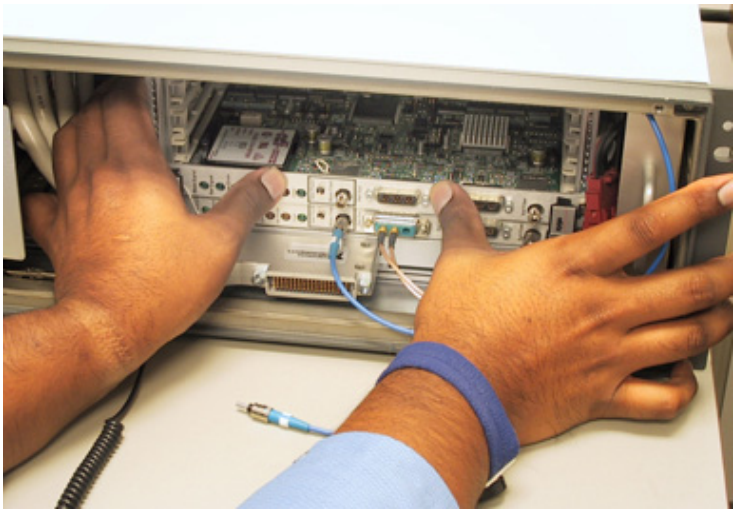
6. Select the P2 Bus base address and SCLK1 Enable with SW5. Each board in the system must have a unique P2 address setting. Select the P2 Bus SCLK swap with JN6.
7. Select the P2 Bus interrupt level for axis 2 with JN7 and axis 1 with JN8.

**Warning!**
Disconnect the VMEbus chassis from power before installing the board and when connecting (or disconnecting) cables.

8. Insert the measurement board into the card cage by pressing on blank areas of the board's front panel with your thumbs to seat the board into the P1 and P2 connectors.

**Figure 2-3** Correct Method of Inserting the Measurement Board in a Card Cage

**Warning!**
Do not install the board with the ejector handles. Pushing on the ejector handles may damage the board.



Actual board may vary from that shown above.

9. Screw the captive front panel screws into the card cage frame.
10. Connect the cables.

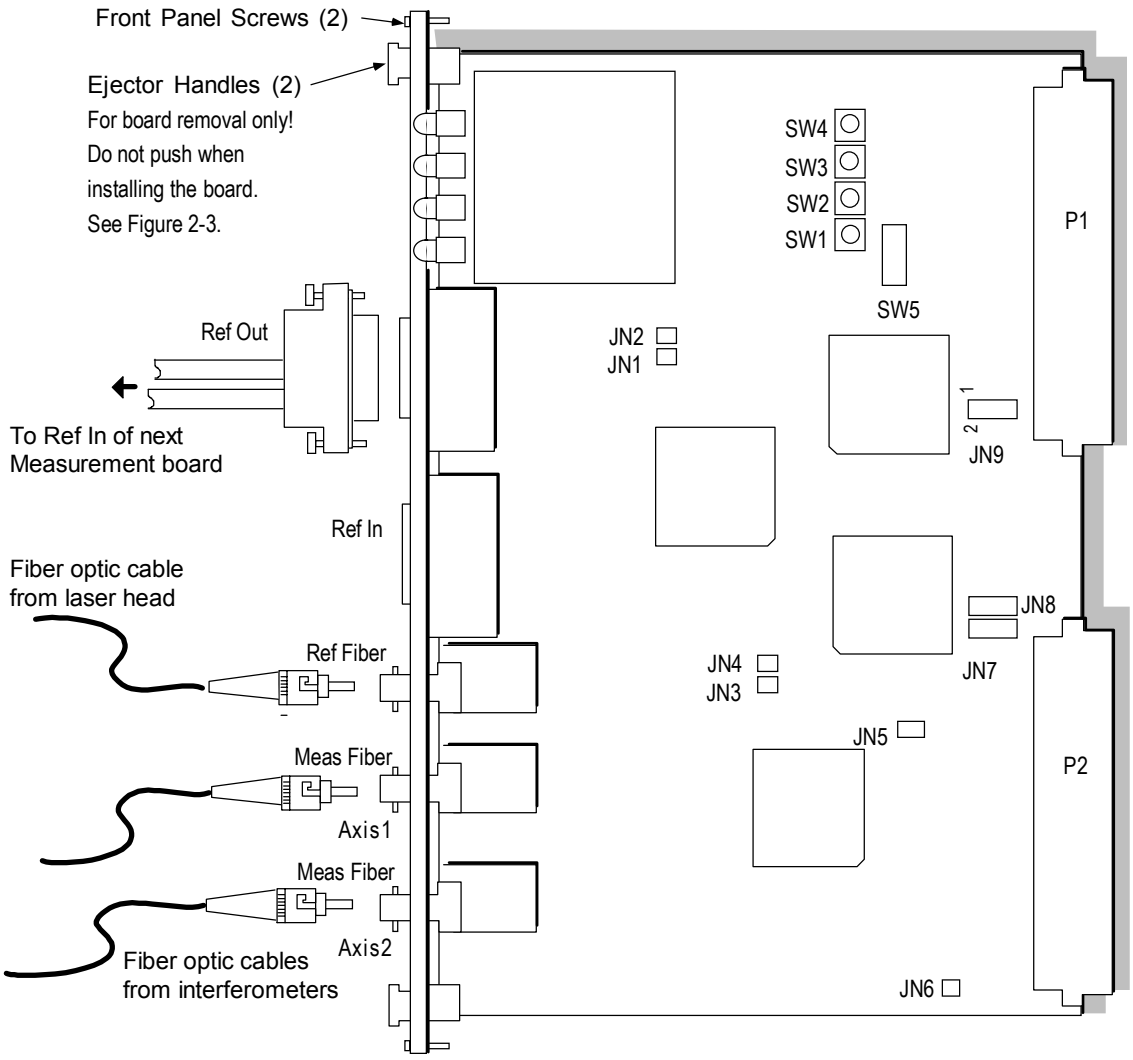



**Figure 2-4** Measurement Board Installation

## VMEbus Base Address Selection

The settings on rotary switches SW1, SW2, SW3, and SW4 determine the VMEbus base address for the Measurement Board. A jumper (JN5) selects A16 or A24 address mode. Each Measurement Board requires a separate 256 byte block of memory in either the A16 or A24 address space. This 256 byte address block must not conflict with the memory map of any other VME boards in the system.

The A16 base address is selected using rotary switches SW3 (MSN) and SW4 (LSN). The A24 base address is selected using switches SW1 (MSN), SW2, SW3, and SW4 (LSN).

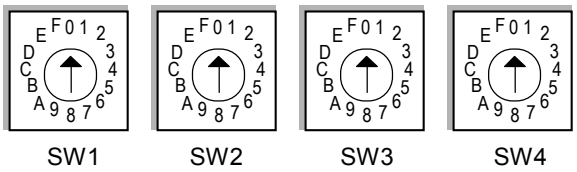



**Figure 2-5** VME Base Address Switches

Measurement Board base addresses are set according to Table 2-2. For example, to set the board to A24 address mode 0x0400, set: SW4-0, SW3-4, SW2-0, and SW1-0.

| *Address Mode* | *JN5 pins* | *Base Address (hexadecimal)* |
|---|---|---|
| **A16** | 4-6 | SW3 SW4 0 0 |
| **A24** | 2-4 | SW1 SW2 SW3 SW4 0 0 |

**Table 2-2** VME Base Address

## VME Interrupt Selection

The Measurement Board can be set for any one of the seven VME interrupt levels. Jumper JN9 sets the interrupt request level. The binary setting written to the Interrupt Vector register, bits 14, 13, and 12 sets the interrupt response level.

**Note:** For proper interrupt selection, set jumper JN9 and the interrupt response level of the Interrupt Vector register, bits 14, 13, and 12 using the VME bus.

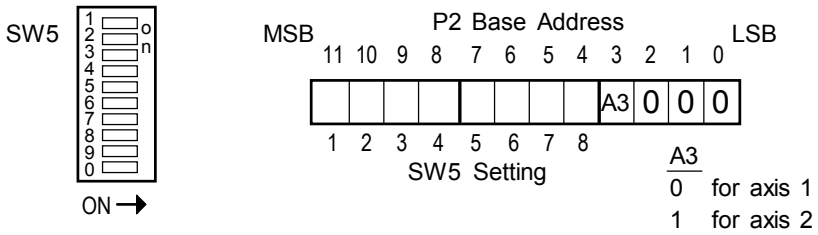
Both levels must be set equal for proper operation. For example, to set the board to interrupt 5, set jumper JN9 to 7-9; and write 101 to the Interrupt Vector register bits 14, 13, and 12.

| *Interrupt Request Level* | *JN9 Jumper Setting* | *Interrupt Vector Register Setting of Bit…* *14* | *13* | *12* |
|---|---|---|---|---|
| off (default state) | 2-4 | 0 | 0 | 0 |
| 1 | 1-3 | 0 | 0 | 1 |
| 2 | 3-5 | 0 | 1 | 0 |
| 3 | 4-6 | 0 | 1 | 1 |
| 4 | 8-10 | 1 | 0 | 0 |
| 5 | 7-9 | 1 | 0 | 1 |
| 6 | 10-12 | 1 | 1 | 0 |
| 7 | 9-11 | 1 | 1 | 1 |

**Table 2-3** VME Interrupt Selection

## *P2 Bus Base Address Selection*

The setting of SW5, switches 1 through 8, determine the P2 Bus base address for the Measurement Board. Switch 1 corresponds to the MSB (bit 11) and switch 8 corresponds to bit 4. Switch on means address bit 0; switch off means address bit 1. The figure below shows the correspondence of the switches to the P2 base address.




**Example**

| *Switch Settings* | *P2 Bus Base Address* |
|---|---|
| on on on on on on on on | 0x000 |
| on off on off on on on on | 0x500 |

**Figure 2-6** P2 Bus Base Address Selection

### *Recommended Grounding*

Improper grounding of the Measurement Board, laser head, or cables may introduce noise in the measurement data. Adhere to the recommendations in Table 2-4 to prevent electromagnetic interference from causing measurement problems.

| *Component* | *Recommendation* |
|---|---|
| Measurement Board | The front panel of the board should be in contact with earth ground through its captive screws. The captive screws secure the board to the card cage, which in turn should be connected to earth ground. |
| Laser Head | The laser head feet and enclosure should be isolated from earth ground. Grounding is provided through the cable. |
| Cables | All cables should be shielded and connected to earth ground through their connectors and the electronic enclosure panel. Use of Zygo supplied cables provides for proper grounding and signal noise immunity. |

**Table 2-4** Grounding Recommendations

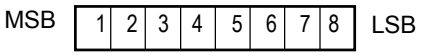
## 2-4 Switch and Jumper Summary

VMEbus settings are shown in Table 2-5. P2 Bus settings are shown in Table 2-6.

| *Switch/Jumper* | *Function* |
|---|---|
| *VMEbus* | |
| SW1 SW2<br>SW3 SW4 | Selects VME A16 or A24 base address (factory default 0000). |
| JN5 | Selects source of board reset signal.<br>pins 1-3 Board reset using VMEbus SYSRESET* signal.<br>pins 3-5 Board reset at power-on (factory default).<br>Selects VMEbus Address mode.<br>pins 2-4 VMEbus A24 address range.<br>pins 4-6 VMEbus A16 address range (factory default). |
| JN9 | Selects VMEbus interrupt level.<br>pins 1-3 VMEbus interrupt request level 1 (IRQ1*).<br>pins 3-5 VMEbus interrupt request level 2 (IRQ2*).<br>pins 4-6 VMEbus interrupt request level 3 (IRQ3*).<br>pins 8-10 VMEbus interrupt request level 4 (IRQ4*).<br>pins 7-9 VMEbus interrupt request level 5 (IRQ5*).<br>pins 10-12 VMEbus interrupt request level 6 (IRQ6*).<br>pins 9-11 VMEbus interrupt request level 7 (IRQ7*).<br>pins 2-4 VMEbus interrupts off (factory default). |

**Table 2-5** VMEbus Switch and Jumper Summary

| *Switch/Jumper* | *Function* |
|---|---|
| *P2 Bus* | |
| SW5 | positions 1-8 P2 Bus base address selection (factory default, all on, address 0x000). |




| position 9 | position 10 | description |
|---|---|---|
| on | on | SCLK1 Disabled (factory default) |
| on | off | SCLK1 Enabled, rising edge |
| off | on | SCLK1 Enabled, both edges (Board rev G and newer) |
| off | on | SCLK1 Disabled (Board rev F and older) |
| off | off | SCLK1 Enabled, falling edge |

JN6 — Selects P2 Bus SCLK0 and SCLK1 exchange.
- pins 1-2 SCLK0 pin input connected to board SCLK0 (factory default).
- pins 3-4 SCLK1 pin input connected to board SCLK1 (factory default).
- pins 1-3 SCLK1 pin input connected to board SCLK0.
- pins 2-4 SCLK0 pin input connected to board SCLK1.

JN7 — Selects P2 Axis 2 Bus Interrupt signal type.
- pins 1-2 Active high TTL level P2 Bus axis 2 interrupt signal.
- pins 3-4 Active low TTL level P2 Bus axis 2 interrupt signal.
- pins 5-6 Open collector driver for P2 Bus axis 2 interrupt (default).

Selects P2 Bus Interrupt signal.
- pins 10-12 Connect axis 2 Interrupt to P2 Bus INT0* signal.
- pins 7-9 Connect axis 2 Interrupt to P2 Bus INT1* signal.
- pins 9-11 Connect axis 2 Interrupt to P2 Bus INT2* signal.
- pins 8-10 Connect axis 2 Interrupt to P2 Bus INT3* signal.
- pins 10-9 Axis 2 P2 Bus interrupt disabled (factory default).

JN8 — Selects P2 Axis 1 Bus Interrupt signal type.
- pins 1-2 Active high TTL level P2 Bus axis 1 interrupt signal.
- pins 3-4 Active low TTL level P2 Bus axis 1 interrupt signal.
- pins 5-6 Open collector driver for P2 Bus axis 1 interrupt (default).

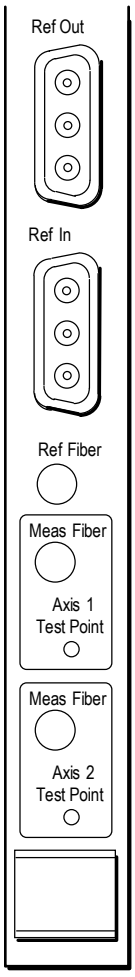
Selects P2 Bus Interrupt signal.
- pins 10-12 Connect axis 1 Interrupt to P2 Bus INT0* signal.
- pins 7-9 Connect axis 1 Interrupt to P2 Bus INT1* signal.
- pins 9-11 Connect axis 1 Interrupt to P2 Bus INT2* signal.
- pins 8-10 Connect axis 1 Interrupt to P2 Bus INT3* signal.
- pins 10-9 Axis 1 P2 Bus interrupt disabled (factory default).

JN1, JN2, JN3, JN4 — For factory use only.

**Table 2-6** P2 Bus Switch and Jumper Summary

## 2-5 Front Panel Connectors

The front panel connectors are summarized in Table 2-7. Additional information on the connectors can be found in the sections that follow.




| *Connector* | *Description* |
|---|---|
| **Ref Out** | Links the reference signal with a daisy chain connection to the next Measurement Board in systems using multiple boards. |
| **Ref In** | Receives an incoming reference signal from another Measurement Board in systems with multiple boards. |
| **Ref Fiber** | Receives incoming reference signal from the laser head through a fiber optic cable. If the system has multiple Measurement Boards, only the first board has an incoming signal from the laser head. |
| **Meas Fiber** | Axis 1. Receives incoming measurement signal from the interferometer through a fiber optic cable. |
| **Test Point** | Axis 1. Provides an output voltage which is used to help optimize the alignment of optical components. |
| **Meas Fiber** | Axis 2. Receives incoming measurement signal from the interferometer through a fiber optic cable. |
| **Test Point** | Axis 2. Provides an output voltage which is used to help optimize the alignment of optical components. |

**Table 2-7** Measurement Board Front Panel Connectors

### *Reference Input (Ref Fiber or Ref In)*

The Measurement Board automatically detects the presence of a reference signal, through either the Ref Fiber or Ref In connector. The reference signal from the Ref In connector (daisy chain input) is used if both Ref Fiber and Ref In are connected. If there is no external reference signal, an internal 20 MHz crystal is used. When several measurement boards are daisy chained together with Ref Out and Ref In connectors, only the first board will reliably detect loss of the reference signal.

### *Meas Fiber and Ref Fiber Connectors*

The Meas Fiber and Ref Fiber connectors are metal fiber optic ST receptacles. A photodiode is located in the back of the receptacle. It is electrically isolated from the front panel, however, it is connected to signal ground on the board.

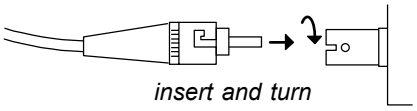
## Connecting Fiber Optic Cables

One or more fiber optic cables can be used to connect the interferometer to the Measurement Board and the Meas Fiber connector. The Zygo Fiber Optic Feed-Thru, P/N 1189-857-076, connects two cables together for extending cable length or for passing through a sheet metal enclosure. The efficiency of each Feed-Thru is typically from 80% to 90%.

**Warning!**
Protective caps should be installed when the cable is not in use. Dropping an unprotected fiber optic cable could damage the fiber.

**Note:** Clearance and bending specifications for fiber optic cables and Fiber Optic Feed-Thru dimensional specifications are located in the ZMI Cable Guide, OMP-0333.

1. Remove protective caps from both ends of fiber optic cable.
2. Examine the fiber end to ensure that no contaminants or reside are present.
3. If necessary, clean the fiber end. Clean the fiber end using a lint free wipe dampened with Methanol or Isopropyl alcohol and gently wipe both cable ends.
4. Insert the cable end into the connector. Align the pin to the slot in the cable's collar. Press and turn the cable clockwise to secure the pin into the cable's detent.




## Ref In and Ref Out Connectors

The Ref In and Ref Out connections use 3C3 subminiature D connectors. The reference daisy chain jumper cable, for jumping the reference signal from one Measurement Board to the next, uses appropriate mating connectors and coaxial cable. This cable assembly is Zygo P/N 1115-801-115.

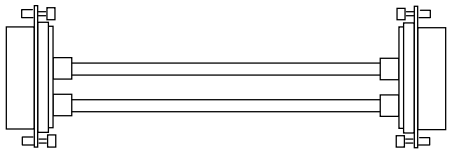
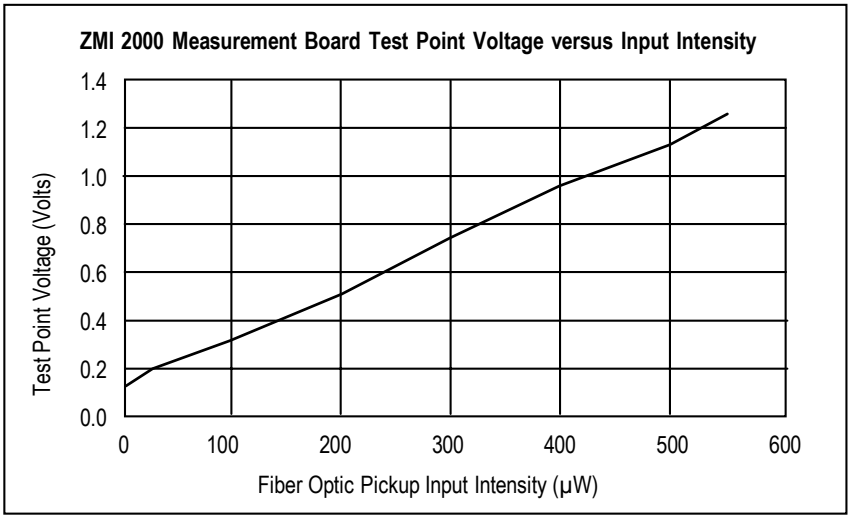


**Figure 2-6** Reference Daisy Chain Jumper Cable

## *Test Point Characteristics*

The Input Intensity refers to the intensity at the Fiber Optic Pickup. The graph shows a typical transfer function characteristic; tolerance on the transfer function is 40% due to Measurement Board component tolerances. In general, the Fiber Optic Pickup position should be adjusted to maximize the front panel test point voltage.




### *Determining if There is Sufficient Optical Signal*

To ensure that there is enough optical signal to satisfy the ZMI 2002 Measurement Board, for the life of the Laser Head, use the following formula:

Good Signal ≥ No signal voltage + (25 mV * Power Factor)

No signal voltage = Front panel test point voltage with fiber optic cable disconnected.

$$\text{Power Factor} = \frac{\text{Current laser head optical power}}{\text{Specified minimum laser head optical power*}}$$

| *Zygo Laser Head P/N | Minimum Power (µW) |
|---|---|
| 6191-0460-01/02/03/04 | 400 |
| 8070-0102-01/02/03/04 | 400 |
| 8070-0102-05 | 500 |

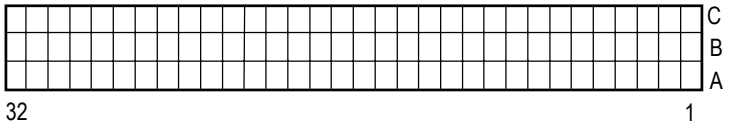
# 2-6 Backplane Connectors

## *P1 Connector and Pin Assignments*

The Measurement Board uses a 96 pin DIN connector (P1) to mate with the VMEbus J1 backplane. This connector complies with the DIN 41612 standard.

**Warning!**
P1 inputs and outputs can be damaged by electrostatic discharge and short circuits in user connections.

**P1 Connector Pin View**




| | *P1 Connector* | | |
|---|---|---|---|
| *Pin* | *Row A* | *Row B* | *Row C* |
| 1 | D0 | not used | D8 |
| 2 | D1 | not used | D9 |
| 3 | D2 | not used | D10 |
| 4 | D3 | not used | D11 |
| 5 | D4 | not used | D12 |
| 6 | D5 | not used | D13 |
| 7 | D6 | not used | D14 |
| 8 | D7 | not used | D15 |
| 9 | GND | not used | GND |
| 10 | not used | not used | not used |
| 11 | GND | not used | not used |
| 12 | DS1* | not used | SYSRESET* |
| 13 | DS0* | not used | LWORD* |
| 14 | WRITE* | not used | AM5 |
| 15 | GND | not used | A23 |
| 16 | DTACK* | AM0 | A22 |
| 17 | GND | AM1 | A21 |
| 18 | AS* | AM2 | A20 |
| 19 | GND | AM3 | A19 |
| 20 | IACK* | GND | A18 |
| 21 | IACKIN* | not used | A17 |
| 22 | IACKOUT* | not used | A16 |
| 23 | AM4 | GND | A15 |
| 24 | A7 | IRQ7* | A14 |
| 25 | A6 | IRQ6* | A13 |
| 26 | A5 | IRQ5* | A12 |
| 27 | A4 | IRQ4* | A11 |
| 28 | A3 | IRQ3* | A10 |
| 29 | A2 | IRQ2* | A9 |
| 30 | A1 | IRQ1* | A8 |
| 31 | not used | not used | not used |
| 32 | +5V | +5V | +5V |

**Table 2-8** P1 Pin Assignment

## P2 Connector and Pin Assignments

The Measurement Board uses a 96 pin DIN connector (P2) to mate with the VMEbus J2 backplane. This connector complies with the DIN 41612 standard. The outer rows of the P2 connector are used for the P2 hardware interface. The pin assignments are shown in Table 2-9.

⚠ **Warnings!**

Unprotected 74ABT125 and 74ABT18245 devices drive P2 output signals. Use recommended termination as described in the next section.

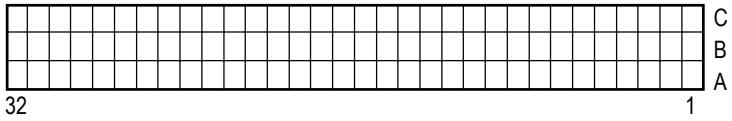
P2 inputs and outputs can be damaged by electrostatic discharge and short circuits in user connections.

Take the following precautions to ensure valid P2 input logic levels:

- The worst case low level input voltage for a logic zero must be less than 0.46 volts.
- Use a common DC ground between the Measurement Board and the source of the external input signal(s).
- Use a signal ground for each external input signal.
- Minimize the length of the interconnecting cable.

## P2 Signal Termination

The P2 Bus is a high speed bus capable of 10 MHz transfer rates under certain conditions. All signals use TTL logic levels. For best results, the P2 backplane should have bussing and termination similar to that provided for the VME backplane. Ribbon cable connections for the P2 bus may work under certain conditions (speed < 1 MHz, total length less than 6 inches, limited to one or two P2 connectors); however, this is neither supported nor recommended by Zygo.




| | *P2 Connector* | | |
|---|---|---|---|
| *Pin* | *Row A* | *Row B* | *Row C* |
| 1 | P2_IOE* | +5V | Reserved |
| 2 | GND | GND | GND |
| 3 | P2_A0 | Reserved | P2_A8 |
| 4 | P2_A1 | Reserved | P2_A9 |
| 5 | P2_A2 | Reserved | P2_A10 |
| 6 | P2_A3 | Reserved | P2_A11 |
| 7 | P2_A4 | Reserved | P2_R/W* |
| 8 | P2_A5 | Reserved | P2_RESET* |
| 9 | P2_A6 | Reserved | GND |
| 10 | P2_A7 | Reserved | Reserved |
| 11 | GND | Reserved | GND |
| 12 | P2_INT0* | GND | P2_INT1* |
| 13 | P2_INT2* | +5V | P2_INT3* |
| 14 | GND | D16 | GND |
| 15 | P2_D16 | D17 | P2_D24 |
| 16 | P2_D17 | D18 | P2_D25 |
| 17 | P2_D18 | D19 | P2_D26 |
| 18 | P2_D19 | D20 | P2_D27 |
| 19 | P2_D20 | D21 | P2_D28 |
| 20 | P2_D21 | D22 | P2_D29 |
| 21 | P2_D22 | D23 | P2_D30 |
| 22 | P2_D23 | GND | P2_D31 |
| 23 | P2_D0 | D24 | P2_D8 |
| 24 | P2_D1 | D25 | P2_D9 |
| 25 | P2_D2 | D26 | P2_D10 |
| 26 | P2_D3 | D27 | P2_D11 |
| 27 | P2_D4 | D28 | P2_D12 |
| 28 | P2_D5 | D29 | P2_D13 |
| 29 | P2_D6 | D30 | P2_D14 |
| 30 | P2_D7 | D31 | P2_D15 |
| 31 | GND | GND | GND |
| 32 | P2_SCLK0 | +5V | P2_SCLK1 |

Notes: P2_A*xx* is P2 address, P2_D*xx* is P2 data, and D*xx* is VME data.

**Table 2-9** P2 Pin Assignment

# *Chapter 3* **Operation**

### *In This Chapter*


3-1 Overview of Measurement Board Operation
3-2 Front Panel Indicators
3-3 VMEbus Data Transfer Modes
3-4 VMEbus Signals
3-5 VMEbus Registers
3-6 P2 Bus Interface Operation
3-7 P2 Bus Signals
3-8 P2 Bus Timing Diagrams
3-9 P2 Bus Registers
3-10 Data Age
3-11 Digital Filtering
3-12 Error Detection and Status Reporting
3-13 Signal Strength Indicator Algorithm


## 3-1 Overview of Measurement Board Operation

The Zygo Measurement Board is a register-based VME card, that supports two measurement axes. As a review, a block diagram of the ZMI-2002 Measurement Board is shown in Figure 3-1. Due to the special functions included in the ZMI-2002, the user must program some parameters using the VMEbus before operating the ZMI.

The board is initialized and all bits in the control registers are cleared when the board receives an active SYSRESET* signal from the VMEbus or when power is turned off and then back on, depending on jumper JN5. After the system is reset, the board responds to A16 bus or A24 cycles, depending on jumper JN5.

When powered up, the laser head takes a number of minutes to stabilize. The Status register's Reference Present bit (bit 0) indicates when the system is ready to make a measurement. It will go high after the laser head stabilizes. The Reset Axis bit in the Command Register (bit 0) should be asserted at this point to clear any errors generated during warm-up.

The user *may* program many register functions during warm-up, such as: Kp and Kv filter settings, Interrupt Vector P2 interrupt control bits, and Data Age Adjust Register bits.

Making measurements with the board consists of accessing the appropriate registers to control interrupts, setting the offset position, sampling and reading the position, velocity, and time. Each register is described in detail later in this chapter.

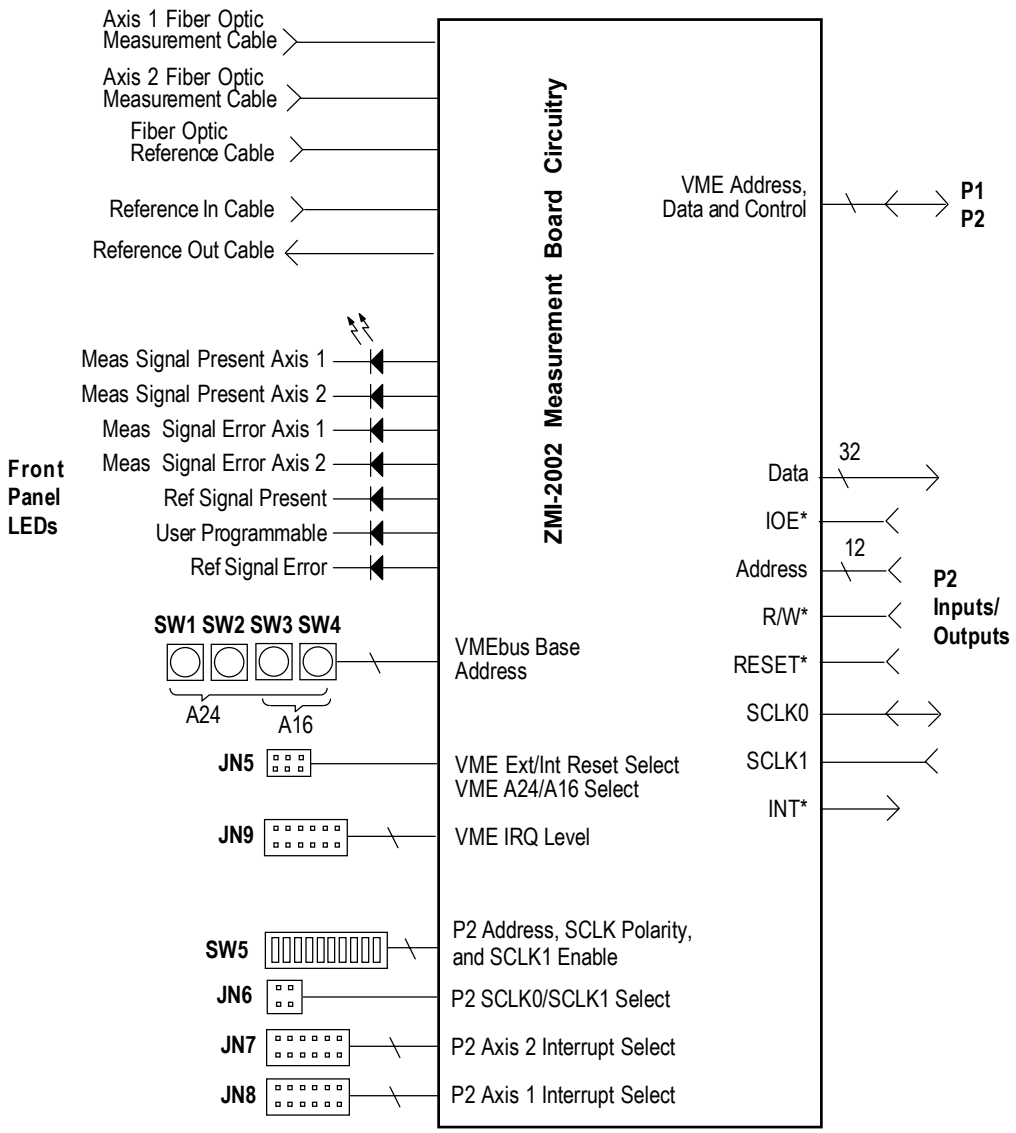
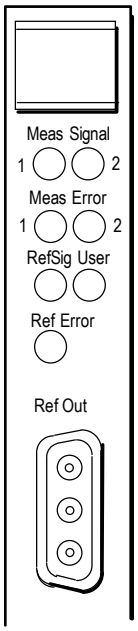



**Figure 3-1** ZMI-2002 Measurement Board Block Diagram

## 3-2 Front Panel Indicators




| *Name* | *Color* | *Description* |
|---|---|---|
| **Meas Signal 1** | Green | Axis 1 measurement signal present. |
| **Meas Signal 2** | Green | Axis 2 measurement signal present. |
| **Meas Error 1** | Yellow | Axis 1 measurement signal missing, measurement signal dropout error, or measurement signal glitch. |
| **Meas Error 2** | Yellow | Axis 2 measurement signal missing, measurement signal dropout error, or measurement signal glitch. |
| **RefSig** | Green | Reference signal present, reference PLL and DLL locked. |
| **User** | Green | User programmable LED (Control Register 1, bit 0, Axis 1). |
| **Ref Error** | Yellow | Reference signal missing error, reference PLL error, or reference DLL error. |

*Note: Errors represented by LED's are the VME Error Register.*

**Figure 3-2** Measurement Board Front Panel Indicators

## 3-3 VMEbus Data Transfer Modes

The Measurement Board is compatible with the following VME data transfer modes:

- A16 or A24 addressing.
- D16 or D32 data transfer.
- D08(O) interrupt acknowledge cycle (RORA).

The Measurement Board also has the following specialized P2 data transfer modes:

- D16 or D32 data transfer.

The board accepts the following Address Modifier codes:

- 0x29 Short Non-Privileged Access.
- 0x2D Short Supervisory Access.
- 0x39 Standard Non-Privileged Access.
- 0x3D Standard Supervisory Access.

## 3-4 VMEbus Signals

The VMEbus signals use the P1 connector; these signals comply with the VMEbus specification, revision C.1 (1987). The P1 connector can supply data as a VME read of 8 bits of 16 bits. For 32-bit VME data, the P2 connector, row B, must be used. This arrangement also conforms to the VMEbus specification.

## 3-5 VMEbus Registers

### *VMEbus Register Address Map*

The ZMI-2002 Measurement Board uses two interface ASICs, one for each measurement axis. Each board has a total of 54 read registers and 30 write registers. The address space is subdivided into axis 1 and axis 2. Both axes operate independently, however, they share a common reference signal. Only axis 1 has an A/D and an EEPROM. Data for both axes is stored in the axis 1 EEPROM. Optical power for both axes are read from the axis 1 interface ASIC A/D.

The user directly accesses the write registers. The read registers are divided into direct access and access through muxed registers. Multiplexing the read registers allows all registers to be mapped into a 32 byte physical address range. This permits Zygo to port this design to other bus structures in the future. The table in Appendix A details the bit locations in all registers.

Muxed read registers are read at offset addresses 0x0C and 0x0E for axis 1 and 0x2C and 0x2E for axis 2. Write registers at these addresses and read/write registers at all other addresses are not muxed. To read a muxed register, the user writes the mux value corresponding to the desired register into the Readback MUX M2, M1, M0 bits in the Interrupt Vector register. The user then reads the corresponding offset address depending on which register is to be read. For example, to read the User Velocity Register on axis 1 the three Readback MUX bits are set to 0, 0, 1, then the User Velocity Register may be read at offset address 0x0E.

The following tables show the address map for the Measurement Board registers. The addresses are relative to the base address selected by the user. The rotary switches, SW1 SW2, SW3, and SW4, select the base address. A jumper (JN5) selects A16 or A24 address mode. See the VMEbus Base Address Selection description in Chapter 2.

| *Offset Location* | *Mux Value* | *Read Registers* | *Write Registers* |
|---|---|---|---|
| 0x1E | NA | Time (LSB) | EEPROM Data |
| 0x1C | NA | Time (MSB) | EEPROM Control |
| 0x1A | NA | Velocity (LSB) | P2 Interrupt Mask |
| 0x18 | NA | Velocity (MSB) | User Excess Velocity |
| 0x16 | NA | Sample Position (LSB) | ADC Mux |
| 0x14 | NA | Sample Position (MSB) | Data Age Adjust |
| 0x12 | NA | Position (LSB) | Offset (LSB) |
| 0x10 | NA | Position (MSB) | Offset (MSB) |
| 0x0E | 6 | Quick Reset High | Offset High Nibbles (redundant w/0x0E Mux 0) |
| 0x0E | 5 | EEPROM Data | Offset High Nibbles (redundant w/0x0E Mux 0) |
| 0x0E | 4 | Data Age Adjust | Offset High Nibbles (redundant w/0x0E Mux 0) |
| 0x0E | 3 | Quick Reset (LSB) | Offset High Nibbles (redundant w/0x0E Mux 0) |
| 0x0E | 2 | Offset (LSB) | Offset High Nibbles (redundant w/0x0E Mux 0) |
| 0x0E | 1 | User Excess Velocity | Offset High Nibbles (redundant w/0x0E Mux 0) |
| 0x0E | 0 | Offset & Position High Nibbles | Offset High Nibbles |
| 0x0C | 5 | P2 Interrupt Mask | Sample Timer (redundant w/0x0C Mux 0) |
| 0x0C | 4 | Phase Meter Diagnostic | Sample Timer (redundant w/0x0C Mux 0) |
| 0x0C | 3 | Quick Reset (MSB) | Sample Timer (redundant w/0x0C Mux 0) |
| 0x0C | 2 | Offset (MSB) | Sample Timer (redundant w/0x0C Mux 0) |
| 0x0C | 1 | Sample Timer | Sample Timer (redundant w/0x0C Mux 0) |
| 0x0C | 0 | Optical Power | Sample Timer |
| 0x0A | NA | Control Register 2 | Control Register 2 |
| 0x08 | NA | Control Register 1 | Control Register 1 |
| 0x06 | NA | Interrupt Vector | Interrupt Vector |
| 0x04 | NA | Error Status | - |
| 0x02 | NA | Interrupt Enable | Interrupt Enable |
| 0x00 | NA | Status Register | Command Register |

NA = not applicable  Reserved = bits for use in other ZMI-2000 board configurations.

**Table 3-1** Axis 1 VMEbus Register Address Map

| *Offset Location* | *Mux Value* | *Read Registers* | *Write Registers* |
|---|---|---|---|
| 0x3E | NA | Time (LSB) | Reserved |
| 0x3C | NA | Time (MSB) | Reserved |
| 0x3A | NA | Velocity (LSB) | P2 Interrupt Mask |
| 0x38 | NA | Velocity (MSB) | User Excess Velocity |
| 0x36 | NA | Sample Position (LSB) | Reserved |
| 0x34 | NA | Sample Position (MSB) | Data Age Adjust |
| 0x32 | NA | Position (LSB) | Offset (LSB) |
| 0x30 | NA | Position (MSB) | Offset (MSB) |
| 0x2E | 6 | Quick Reset High | Offset High Nibbles (redundant w/0x2E Mux 0) |
| 0x2E | 5 | Reserved | Offset High Nibbles (redundant w/0x2E Mux 0) |
| 0x2E | 4 | Data Age Adjust | Offset High Nibbles (redundant w/0x2E Mux 0) |
| 0x2E | 3 | Quick Reset (LSB) | Offset High Nibbles (redundant w/0x2E Mux 0) |
| 0x2E | 2 | Offset (LSB) | Offset High Nibbles (redundant w/0x2E Mux 0) |
| 0x2E | 1 | User Excess Velocity | Offset High Nibbles (redundant w/0x2E Mux 0) |
| 0x2E | 0 | Offset & Position High Nibbles | Offset High Nibbles |
| 0x2C | 5 | P2 Interrupt Mask | Reserved (redundant w/0x2C Mux 0) |
| 0x2C | 4 | Phase Meter Diagnostic | Reserved (redundant w/0x2C Mux 0) |
| 0x2C | 3 | Quick Reset (MSB) | Reserved (redundant w/0x2C Mux 0) |
| 0x2C | 2 | Offset (MSB) | Reserved (redundant w/0x2C Mux 0) |
| 0x2C | 1 | Reserved | Reserved (redundant w/0x2C Mux 0) |
| 0x2C | 0 | Reserved | Reserved |
| 0x2A | NA | Control Register 2 | Control Register 2 |
| 0x28 | NA | Control Register 1 | Control Register 1 |
| 0x26 | NA | Interrupt Vector | Interrupt Vector |
| 0x24 | NA | Error Status | - |
| 0x22 | NA | Interrupt Enable | Interrupt Enable |
| 0x20 | NA | Status Register | Command Register |

NA = not applicable  Reserved = bits for use in other ZMI-2000 board configurations.

**Table 3-2** Axis 2 VMEbus Register Address Map

## *Command Register*
## (Axis 1, 0x00 write only) (Axis 2, 0x20 write only)

The Command Register is a write only register; it is used for general system operation. Setting a command bit high causes the indicated action. The bits are automatically cleared (re-enabled) after the action is taken.

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0 | Reset axis | Resets the digital filter, position accumulator, Time register, and all VME and P2 errors. May take up to 25 milliseconds depending on Kp and Kv, and reset time delay (Control Register 2). User must execute this command or a power-on reset to clear any fatal errors. This command is complete when the position reset complete bit (bit 4) in the Status Register is set. |
| 4 | Reset position | Resets the digital filter and position accumulator. May take up to 25 milliseconds depending on Kp and Kv, and reset time delay (Control Register 2). This command is complete when the position reset complete bit (bit 4) in the Status Register is set. |
| 5 | Quick position reset | Forces the position value to 0 by saving the current value, then subtracting it from all following position reads. This action is before the value in the Offset Register is subtracted from the position. |
| 6 | Reset time | Resets the time register. |
| 7 | Reset user velocity error | Resets the user velocity error. This error occurs when the most significant 16 bits of the velocity exceed the 16 bit value stored in the User Excess Velocity register. The user velocity error bit will be set again if the velocity continues to exceed the User Excess Velocity value even after this reset command is issued. |
| 8 | Force external sample (SCLK0) (Axis 1 only) | When P2 SCLK0 clock is disabled (Control Register 1, bit 10), this outputs a pulse on the P2 interface external sample output (SCLK0). For this to produce the output, the P2 SCLK0 output enable bit (Control Register 1, bit 11) must be set. When P2 SCLK0 clock is enabled, this function is disabled. |
| 9 | Sample VME position | Forces the VME position, velocity, time, and data registers to latch the current values. In revision A ASIC, this function is disabled if trigger delay is enabled (Control Register 2, bit 11). |
| 10 | Reset 32 bit position overflow | Resets the 32 bit position overflow error. This error occurs when the position value exceeds the user selected 32 bit window into the 36 bit position accumulator. |
| 11 | Reset P2 SCLK0 interrupt | Resets the P2 external sample (SCLK0) condition that generated a VMEbus interrupt. |

**Table 3-3** Command Register Actions

## *Status Register*
## (Axis 1, 0x00 read only) (Axis 2, 0x20 read only)

The Status Register is read only; it provides instantaneous board operations status. The user reads these signals during system initialization to verify the presence of valid measurement and reference signals. For example, the user may read the reference present bit to determine if the laser head has completed its warm-up cycle.

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0 | Reference present | Indicates that the reference signal is present. |
| 1 | Reference PLL | Indicates that the reference PLL is locked. |
| 2 | Reference DLL | Indicates that the reference DLL is locked. |
| 3 | Measure present | Indicates that the measure signal is present. |
| 4 | Position reset complete | Indicates that the reset position command has been completed. This bit stays on until the next position reset or reset axis command is executed. |
| 5 | ADC ready (Axis 1 only) | Indicates that a valid A/D converter value is present in the Optical Power register. Stays on until new ADC mux value is written. |
| 6 | ADC Mux=0 (Axis 1 only) | Indicates that the A/D converter mux is set to measure the optical power signal. |
| 7 | EEPROM busy (Axis 1 only) | High while EEPROM is accessing requested data. When it returns low, the data is available in the EEPROM Data Read Register (0x0E Mux 5). |
| 8 | External sample flag (SCLK0) | Indicates that the external sample (SCLK0) command has been received. |
| 9-14 | reserved | Factory use only. |
| 15 | Version | This bit is zero in revision A interface ASIC and one in revision B ASIC. The differences between the two versions are described in this manual when applicable. |

**Table 3-4** Status Register Functions

### *Interrupt Enable Register*
### (Axis 1, 0x02 read/write) (Axis 2, 0x22 read/write)

The Interrupt Enable Register is a read/write register which specifies the error conditions that generate VMEbus interrupts. It also includes the VMEbus interrupt inhibit bit. The user writes a 1 into the bit locations corresponding to the desired interrupt generating errors. All interrupt enable bits are set to 0 (disabled) during the power-on reset.

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0 | Reference signal missing | Generates an interrupt when the reference signal is missing. |
| 1 | Reference PLL error | Generates an interrupt when the reference PLL is not locked. |
| 2 | Reference DLL error | Generates an interrupt when the reference DLL is not locked. |
| 3 | Measure signal missing | Generates an interrupt when the measurement signal is missing. |
| 4 | Measure signal dropout | Generates an interrupt when the measurement signal momentarily drops out. |
| 5 | Measure signal glitch | Generates an interrupt when the phase meter ASIC detects a second edge on the measurement signal within a 40 MHz clock period. |
| 6 | Velocity error | Generates an interrupt when a velocity error is detected. |
| 7 | User velocity error | Generates an interrupt when the most significant 16 bits of the velocity exceed the 16 bit value stored in the User Excess Velocity Register. |
| 8 | Acceleration error | Generates an interrupt when an acceleration error occurs. |
| 9 | 36 bit position overflow | Generates an interrupt when the 36 bit position value overflows. |
| 10 | 32 bit position overflow | Generates an interrupt when the position value exceeds the user selected 32 bit window into the 36 bit position accumulator. |
| 11 | P2 external sample (SCLK0) | Generates an interrupt when an external sample is detected. |
| 15 | Interrupt inhibit | Enables/disables VMEbus interrupts. Power-on default is disabled. |

**Table 3-5** Interrupt Enable Register Functions

## *Error Status Register*
## (Axis 1, 0x04 read only) (Axis 2, 0x24 read only)

The Error Status Register is a read only register which indicates the current error condition status. This register latches momentary errors, such as measure signal glitch, so that the user can detect these conditions. The error status latches are reset after a SYSRESET* active signal or a reset axis command. The user velocity error, the 32 bit position overflow error, and the P2 external sample flag may be individually reset.

See the Error Detection and Status Reporting" Section later in this chapter for the structure of this register.

| *Bit* | *Signal* | *Description* |
|---|---|---|
| 0* | Reference signal missing | See "Error Detection and Status Reporting". |
| 1* | Reference PLL error | See "Error Detection and Status Reporting". |
| 2* | Reference DLL error | See "Error Detection and Status Reporting". |
| 3* | Measure signal missing | See "Error Detection and Status Reporting". |
| 4* | Measure signal dropout | See "Error Detection and Status Reporting". |
| 5* | Measure signal glitch | See "Error Detection and Status Reporting". |
| 6* | Velocity error | See "Error Detection and Status Reporting". |
| 7 | User velocity error | See "Error Detection and Status Reporting". |
| 8* | Acceleration error | See "Error Detection and Status Reporting". |
| 9* | 36 Bit position overflow | See "Error Detection and Status Reporting". |
| 10 | 32 Bit position overflow | See "Error Detection and Status Reporting". |
| 11 | P2 external sample (SCLK0) | Indicates that an external sample has occurred. This bit can be reset with the reset P2 SCLK0 interrupt bit (Command Register, bit 11). |
| 15 | IRQ pending | Indicates a pending VME interrupt. |

* These errors are considered "fatal" errors and stop updates of the Position Register unless the disable excess velocity bit (Control Register 2, bit 15) is set.

**Table 3-6** Error Status Register Functions

### *Interrupt Vector Register*
### (Axis 1, 0x06 read/write) (Axis 2, 0x26 read/write)

The Measurement Board compares the CPU interrupt level indicated during an interrupt acknowledge cycle to the value stored in bits 12, 13, and 14 of the Interrupt Vector register. If the values are equal, then the board responds to the interrupt acknowledge cycle by placing the interrupt vector on the data bus. The interrupt vector is stored in bits 0-7 of the Interrupt Vector Register. The user programs bits 8-10 to select muxed read registers. Bit 15 is reserved for factory testing.

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0-7 | Interrupt Vector | Value placed on the VME data bus by the board during an interrupt acknowledge cycle. |
| 8-10 | Readback MUX bits | Three bit value used to access the muxed read registers at offset addresses 0x0C and 0x0E. |
| 12-14 | Interrupt Level | Three bit interrupt level value used by the board to determine if it should acknowledge the current CPU interrupt cycle. |
| 15 | Factory Test | Reserved for factory use only. This bit should always be 0. |

**Table 3-7** Interrupt Vector Register Functions

### *Control Register 1*
### (Axis 1, 0x08 read/write) (Axis 2, 0x28 read/write)

Control Register 1 is a read/write register. The user programs various bits in the register to select the desired options. The functions for Control Register 1 are summarized in Table 3-9.

The position bit window (bits 12-14) determine which 32 bits are output. The 32 bit position data window permits the user to perform one VMEbus 32 bit read cycle to receive the desired position data. The user selects 32 of the total 36 position bits depending on the position resolution required by the user's system. The desired 32 bits are selected by writing a 3 bit binary value into bits 12, 13, and 14 of Control Register 1. The power-on default is 0, 0, 0. A programming example for position bit window selection is shown below.

| *Control Register 1 Bits* | | | *Position Bits Selected* |
|---|---|---|---|
| *14* | *13* | *12* | *32 Bit Window* |
| 0 | 0 | 0 | P31 - P0 |
| 0 | 0 | 1 | P32 - P1 |
| 0 | 1 | 0 | P33 - P2 |
| 0 | 1 | 1 | P34 - P3 |
| 1 | 0 | 0 | P35 - P4 |

**Table 3-8** Position Bit Window Selection

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0 | User LED (Axis 1 only) | Controls the user LED on the front panel. The power-on default status is off. |
| 1 | User P2 | Controls the user bit in the P2 error/status/high nibble register. The power-on default value is 0. |
| 2 | Factory Test | This bit should always be 0. |
| 3 | P2 RESET - error reset enable | Allows the P2 error reset function to operate when the P2 interface RESET* signal is active. The power-on default condition is disabled (0). This resets the P2 Error Register, but has no effect on the VME Error Status Register. |
| 4 | P2 RESET - position enable | Allows the position reset function (as described for Command Register, bit 4) to operate when the P2 interface RESET* signal is active. The power-on default condition is disabled (0). |
| 5 | P2 RESET - quick reset enable | Allows the quick reset function (as described for Command Register, bit 5) to operate when the P2 interface RESET* signal is active. The power-on default condition is disabled (0). |
| 6 | P2 RESET - time reset enable | Allows the time reset function (as described for Command Register, bit 6) to operate when the P2 interface RESET* signal is active. The power-on default condition is disabled (0). |
| 7 | Reserved | Always set to zero (0). |
| 8 | P2 latch mode | A 0 selects the P2 interface external sample (SCLK0) input or a 1 selects the P2 position read as the method for latching data into the P2 register. The power-on default value is SCLK0 input (0). |
| 9 | P2 D16 select | Selects between a 16 or 32 bit data path for the P2 interface. Program this bit with a 1 to select the D16. The power-on default value is 0 (32 bits). |
| 10 | P2 SCLK0 clock disable (Axis 1 only) | Disable the P2 SCLK0 sample clock. The power-on default value is clock enabled (0). The period of this clock is controlled by the Sample Timer Register. |
| 11 | P2 SCLK0 output enable (Axis 1 only) | Enables the P2 SCLK0 output to the bus. The power-on default value is output disabled (0). |
| 12-14 | Position bit window A0, A1, A2 | Selects which 32 of the 36 bit position is output to the least significant 32 bits of the position registers. This always controls the P2 data and optionally controls the VME data depending on the setting of bit 15, VME bit window enable. The power on default value is 0,0,0. (See Table 3-8.) |
| 15 | VME bit window enable | Selects the source of the least significant 32 position register bits for the VME outputs, either from the shifter or directly from the position accumulator. See Figure 4-7 for a block diagram. |

**Table 3-9** Control Register 1 Functions

## *Control Register 2*
## (Axis 1, 0x0A read/write) (Axis 2, 0x2A read/write)

Control Register 2 is a read/write register. The user programs various bits in the register to select the desired options.

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0-2 | Kv | Three bit value which represents the digital filter Kv gain value. See the Digital Filtering section in this Chapter for the valid gain values. |
| 3 | reserved | Factory use only. |
| 4-6 | Kp | Three bit value which represents the digital filter Kp gain value. See the Digital Filtering section in this Chapter for the valid gain values. |
| 7 | reserved | Factory use only. |
| 8-10 | Reset time bits RT0, RT1, RT2 | Programmable delay indicating when the position reset command is complete. Power-on default 0, 0, 0. See the following table. |
| 11 | Trigger delay enable | Enables a circuit to delay position latching caused by an external SCLK0 sample signal. This reduces the effective pipeline delay. |
| 12 | Enable 32-bit overflow | (Rev. B ASIC only) Allows the detection of 32-bit overflows. This is only useful if both the VME and P2 interfaces are using only 32 bits. |
| 13 | reserved | Factory use only. This bit should always be 0. |
| 14 | Change position direction sense | Setting this bit reverses the direction sense of the position accumulator. Must execute a position reset or axis reset after changing the direction sense. |
| 15 | Disable Excess Velocity | The velocity errors (Error Status Register, bit 6; and P2 Error Register, bit 27) are disabled if this bit is 1. |

**Table 3-10** Control Register 2 Functions

| *Reset Time* | | | *Reset Delay* |
|---|---|---|---|
| *RT2* | *RT1* | *RT0* | |
| 0 | 0 | 0 | 2 µs |
| 0 | 0 | 1 | 6 µs |
| 0 | 1 | 0 | 26 µs |
| 0 | 1 | 1 | 102 µs |
| 1 | 0 | 0 | 410 µs |
| 1 | 0 | 1 | 1.6 ms |
| 1 | 1 | 0 | 6.5 ms |
| 1 | 1 | 1 | 26.2 ms |

**Table 3-11** Reset Time Delay

## *Optical Power Register*
## (Axis 1 only, 0x0C Mux 0 read only)

A number corresponding to the measurement signal optical power is available on bits 0-9 of the Optical Power Register (read only). This register is accessed through the muxed register set. The value is read from an on-board 10 bit A/D converter. It has a range of 0 to 1023 which corresponds to 0 to 2.5 volts at the A/D converter. The A/D converter is part of the fiber optic measurement receiver circuit. The A/D converter MUX must be set to 0 (power-on default state) to read the measurement signal optical power.

The interface ASIC continuously reads the A/D converter. The user may read the voltage at another A/D mux input by writing the desired A/D mux value to the VMEbus ADC MUX Register. The ADC Ready bit in the Status Register indicates when the A/D converter result from the new mux value can be read.

For diagnostic purposes, several on-board voltages can be measured with the ADC (Analog-to-Digital Converter). Full scale on the ADC (0x3FF) corresponds to 2.495V at the selected input pin. The ADC inputs and overall tolerances are listed below. $N_{ADC}$ is the value read from the ADC.

| *ADC Mux* | *Description* |
|---|---|
| 0 | Measurement 1 Signal power (±2.2%).<br>$V_{SSI} = N_{ADC} * 0.00244$ |
| 1 | Measurement 2 Signal power (±2.2%).<br>$V_{SSI} = N_{ADC} * 0.00244$ |
| 2 | Measurement 1 detector bias voltage (±4.0% ±0.25V).<br>$V_{MBias} = N_{ADC} * 0.0268$ |
| 3 | Measurement 2 detector bias voltage (±4.0% ±0.25V).<br>$V_{MBias} = N_{ADC} * 0.0268$ |
| 4 | Phase Meter ASIC 1 thermal diode voltage (±2.2%).<br>$THDIODE = N_{ADC} * 0.00244$ |
| 5 | Phase Meter ASIC 2 thermal diode voltage (±2.2%).<br>$THDIODE = N_{ADC} * 0.00244$ |
| 6 | Reference detector bias voltage (±4.0% ±0.25V).<br>$V_{Bias} = N_{ADC} * 0.0268$ |
| 7 | 24 Volt bias supply (±4.0% ±0.25V).<br>$V_{Bias} = N_{ADC} * 0.0268$ |
| 8 | 5 Volt analog power supply (±3.3%).<br>$VCC3 = N_{ADC} * 0.00547$ |
| 9 | 5 Volt digital power supply (±3.3%).<br>$VCC = N_{ADC} * 0.00547$ |
| 10-13 | Factory use. |

**Table 3-12** ADC Inputs

### *Sample Timer Register*
### (Axis 1 only, 0x0C write, 0x0C Mux 1 read)

The Sample Timer Register value controls the P2 external sample clock (SCLK0) frequency. The user writes a sample timer value to offset address 0x0C. The user can read back the value by reading one of the muxed register locations. The power-on default is 0x0007.

The period of the sample clock in nanoseconds is:

$$\text{period} = (n + 1)*50 \text{ nsec} \quad \text{for } 0 \leq n \leq 65535$$

Where n equals the value programmed into register. For example, to latch the P2 interface position data at a 5 kHz rate, the user must program the Sample Timer Register with 3999.

For the sample timer to operate, Control Register 1, bit 10 (P2 SCLK0 disable) must be 0. For the sample timer to drive the P2 bus, Control Register 1, bit 11 (P2 SCLK0 output enable) must be 1.

### *Offset Register*
### (Axis 1, 0x10-0x12 write, 0x0C-0x0E Mux 2 read)
### (Axis 2, 0x30-0x32 write, 0x2C-0x2E Mux 2 read)

The Offset Register is the 32 bit value used in conjunction with the high offset nibbles in the High Nibbles Register to program the position offset value. All 36 bits are latched into the Offset Register when the least significant word is written. The value in the Offset Register is subtracted from the position value. The read and write offset address locations are different. The user can read back the value by reading muxed register locations.

To preset the position value, load the Offset Register with the negation of the desired preset value, then execute a position reset. The position value read after the reset function is complete will equal the negated contents of the offset register.

### *Quick Reset Register*
### (Axis 1, 0x0C Mux 3, 0x0E Mux 3, 0x0E Mux 6, read only)
### (Axis 2, 0x2C Mux 3, 0x2E Mux 3, 0x2E Mux 6, read only)

The user can read back the value saved by a quick reset operation by reading one of the muxed register locations. The resolution of this register is 1/8 LSB. This register is intended for factory diagnostic use only.

### *High Nibbles Registers*
### (Axis 1, 0x0E write, 0x0E Mux 0 read)
### (Axis 2, 0x2E write, 0x2E Mux 0 read)

The High Nibbles Register allows the user to read the upper 4 bits of the 36 bit Offset, Position, and Sample Position registers. It also allows the user to program the upper 4 bits of the offset register. The read and write locations are different. The user can read back these bits by reading one of the muxed register locations.

| *Bits* | *Register* |
|---|---|
| 0-3 | Position (read only) |
| 4-7 | Sample Position (read only) |
| 8-11 | not used |
| 12-15 | Offset |

**Table 3-13** Bit Locations in Offset Register

### *User Excess Velocity Register*
### (Axis 1, 0x18 write, 0x0E Mux 1 read)
### (Axis 2, 0x38 write, 0x2E Mux 1 read)

For Measurement Boards with revision A ASIC's, the user must program this register to an appropriate value or a user velocity error is generated. If this function is not used program the value to 0xFFFF. For boards with revision B ASIC's, the register defaults to 0xFFFF at power-up.

If the absolute value of the most significant 16 bits of the velocity exceed the 16 bit value stored in this register, then the user excess velocity error bit is set. The error bit will remain set until the user writes a 1 to the reset user velocity error bit in the Command Register or performs a reset axis. The power-on default value for this register is 0xFFFF.

The read and write locations are different. The user can read back these bits by reading one of the muxed register locations.

### *Data Age Adjust Register*
### (Axis 1, 0x14 write, 0x0E Mux 4 read)
### (Axis 2, 0x34 write, 0x2E Mux 4 read)

The Data Age Adjust Register is a read/write register. It is used to store a compensated data age value, which is later read. See the "Data Age" section later in this chapter.

Bits 14 and 15 contain data related to the Phase Meter Diagnostic Register.

### *Phase Meter Diagnostic Register*
### (Axis 1, 0x0C Mux 4, read only)
### (Axis 2, 0x2C Mux 4, read only)

Two consecutive phase values directly from the phase meter can be read after being latched by the sample VME position command. This can be used for measuring the data age. The use of this register to verify data age compensation is described in the "Data Age" section later in this chapter.

Register 0x0C Mux 4 contains the lower 8 bits of two 9-bit phase values. Register 0x0E Mux 4 contains the $9^{th}$ bits of the two phase values.

Phase value A = (0x0E Mux 4, bit 14) (0x0C Mux 4 bits 7-0)
Phase value B = (0x0E Mux 4, bit 15) (0x0C Mux 4 bits 15-0)

### *EEPROM Control Register*
### (Axis 1 only, 0x1C write only)

### *EEPROM Read Data Register*
### (Axis 1 only, 0x0E Mux 5 read only)

### *EEPROM Write Data Register*
### (Axis 1 only, 0x1E write only)

The EEPROM Control and EEPROM Data registers are used to read data from the onboard serial EEPROM. The EEPROM is factory pre-programmed with data age and signal strength information.

The EEPROM on board versions A and B is shown in Table 3-14. The EEPROM on board revisions C and later is shown in Table 3-15.

The board type and board revision are in the same location in all EEPROM's, and must be read to determine which data structure is used. To read information from EEPROM, the user writes the EEPROM command, address, and mode bits into the EEPROM Control register. The interface ASIC takes this information and sends it serially to the EEPROM, then reads the serial data from the device, storing it in the EEPROM Read Data Register. The user must wait until the EEPROM busy bit (Status Register) returns low before reading data from the EEPROM Read Data Register.

Bits 8 through 15 of the EEPROM Control Register are always set to 0 for the read operation. Bits 6 and 7 are always set to 0 and 1 respectively. Bits 0 through 5 are programmed with the EEPROM register address.

For example, to read EEPROM register 0x02:

1. Write 0x080 + 0x02 = 0x082 into the EEPROM Control Register at offset address 0x1C.
2. Wait until EEPROM busy returns low.
3. Set the Readback MUX bits in the Interrupt Vector Register to 0x05.
4. Read the EEPROM Data Register at offset address 0x0E.

## EEPROM Data Register

The memory and bit locations of information in the EEPROM Data Register is described in the following tables. Board versions B and earlier start below.

| *Address* | *Bit Description* |
|---|---|
| 0x0 | Bits 0-15, Serial number of Measurement Board. |
| 0x1 | Bits 0-4, Day of manufacture. Bits 5-8, Month of manufacture.<br>Bits 9-12, Year of manufacture, add 1996 to this 4-bit value to determine the year.<br>Bits 13-15, Measurement Board model code, 000 = ZMI-2001, 001 = ZMI-2002. |
| 0x2 | Bits 0-11, Board assembly revision, two 6-bit characters; add 32 to each 6-bit value to convert to ASCII characters.<br>Bits 12-15, Board assembly configuration number, 0001 = -01 configuration. |
| 0x3 | Bits 0-9, Value of VCC3 power supply voltage as measured during factory test.<br>Bits 10-12, Signal strength indicator (SSI) algorithm version; this value determines which SSI algorithm should be used with the SSI values stored in memory.<br>Bits 13-15, Data age compensation algorithm version; this value determines which data age compensation algorithm should be used with the stored data age values. |
| 0x4 | Bits 0-5, Reference daisy chain delay value for use with the data age compensation algorithm.<br>Bits 6-15, Axis 1 measurement signal detector bias voltage (no signal) as measured during factory test. |
| 0x5 | Bits 0-7, Axis 1 signal strength indicator (SSI) A/D value for point 0; this value correspond to zero optical power; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 1 measurement channel delay value used with the data age compensation algorithm. |
| 0x6 | Bits 0-7, Axis 1 signal strength indicator (SSI) A/D value for point 1; this value corresponds to the optical power at point 1; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 1 signal strength indicator (SSI) optical power for point 1; this is the optical power input to the measurement receiver to obtain the A/D value. |
| 0x7 | Bits 0-7, Axis 1 signal strength indicator (SSI) A/D value for point 2; this value multiplied by 4 corresponds to the optical power at point 2; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 1 signal strength indicator (SSI) optical power for point 2; this is the optical power input to the measurement receiver to obtain the A/D value. |
| 0x8 | Bits 0-7, Axis 1 signal strength indicator (SSI) A/D value for point 3; this value multiplied by 4 corresponds to the optical power at point 3; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 1 signal strength indicator (SSI) optical power for point 3; this value multiplied by 4 is the optical power input to the measurement receiver to obtain the A/D value. |
| 0x9 | Bits 0-9, Axis 1 signal strength indicator (SSI) A/D value for point 4; this value multiplied by 4 corresponds to the optical power at point 4; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 10-15, Axis 1 signal strength indicator (SSI) optical power for point 4; this value multiplied by 4 is the optical power input to the measurement receiver to obtain the A/D value. |

*continued*

**Table 3-14** EEPROM Data Register Bit Locations (Rev B and earlier)

| *Address* | *Bit Description* |
|---|---|
| 0xA | Bits 0-5, Reference daisy chain delay value for use with the data age compensation algorithm.<br>Bits 6-15, Axis 2 measurement signal detector bias voltage (no signal) as measured during factory test. |
| 0xB | Bits 0-7, Axis 2 signal strength indicator (SSI) A/D value for point 0; this value correspond to zero optical power; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 2 measurement channel delay value used with the data age compensation algorithm. |
| 0xC | Bits 0-7, Axis 2 signal strength indicator (SSI) A/D value for point 1; this value corresponds to the optical power at point 1; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 2 signal strength indicator (SSI) optical power for point 1; this is the optical power input to the measurement receiver to obtain the A/D value. |
| 0xD | Bits 0-7, Axis 2 signal strength indicator (SSI) A/D value for point 2; this value multiplied by 4 corresponds to the optical power at point 2; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 2 signal strength indicator (SSI) optical power for point 2; this is the optical power input to the measurement receiver to obtain the A/D value. |
| 0xE | Bits 0-7, Axis 2 signal strength indicator (SSI) A/D value for point 3; this value multiplied by 4 corresponds to the optical power at point 3; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 2 signal strength indicator (SSI) optical power for point 3; this value multiplied by 4 is the optical power input to the measurement receiver to obtain the A/D value. |
| 0xF | Bits 0-9, Axis 2 signal strength indicator (SSI) A/D value for point 4; this value multiplied by 4 corresponds to the optical power at point 4; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 10-15, Axis 2 signal strength indicator (SSI) optical power for point 4; this value multiplied by 4 is the optical power input to the measurement receiver to obtain the A/D value. |

**Table 3-14** EEPROM Data Register Bit Locations (Rev B and earlier) (continued)

| *Address* | *Bit Description* |
|---|---|
| 0x0 | Bits 0-15, reserved. |
| 0x1 | Bits 0-4, Day of manufacture. Bits 5-8, Month of manufacture.<br>Bits 9-12, Year of manufacture, add 1996 to this 4-bit value to determine the year.<br>Bits 13-15, Measurement Board model code, 000 = 2001, 001 = 2002, 010 = 2004, 011 = 2004A. |
| 0x2 | Bits 0-11, Board assembly revision, two 6-bit characters; add 32 to each 6-bit value to convert to ASCII characters.<br>Bits 12-15, Board assembly configuration number, 0001 = -01 configuration. |
| 0x3 | Bits 0-15, Serial number of Measurement Board LSB. |
| 0x4 | Bits 0-15, Serial number of Measurement Board MSB. |
| 0x5 | Bits 0-9, Value of VCC3 power supply voltage as measured during factory test.<br>Bits 10-12, Signal strength indicator (SSI) algorithm version; this value determines which SSI algorithm should be used with the SSI values stored in memory.<br>Bits 13-15, Data age compensation algorithm version; this value determines which data age compensation algorithm should be used with the stored data age values. |
| 0x6 | Bits 0-5, Reference daisy chain delay value for use with the data age compensation algorithm.<br>Bits 6-15, Axis 1 measurement signal detector bias voltage (no signal) as measured during factory test. |
| 0x7 | Bits 0-7, Axis 1 signal strength indicator (SSI) A/D value for point 0; this value correspond to zero optical power; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 1 measurement channel delay value for use with the data age compensation algorithm. |
| 0x8 | Bits 0-15, Axis 1 signal strength indicator (SSI) A/D value for point 1; this value corresponds to the optical power at point 1; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0x9 | Bits 0-15, Axis 1 signal strength indicator (SSI) optical power for point 1; this is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0xA | Bits 0-15, Axis 1 signal strength indicator (SSI) A/D value for point 2; this value corresponds to the optical power at point 2; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0xB | Bits 0-15, Axis 1 signal strength indicator (SSI) optical power for point 2; this is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0xC | Bits 0-15, Axis 1 signal strength indicator (SSI) A/D value for point 3; this value corresponds to the optical power at point 3; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0xD | Bits 0-15, Axis 1 signal strength indicator (SSI) optical power for point 3; this value is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0xE | Bits 0-15, Axis 1 signal strength indicator (SSI) A/D value for point 4; this value corresponds to the optical power at point 4; use this value with the SSI algorithm to determine the optical power of the measurement signal. |

*continued*

**Table 3-15** EEPROM Data Register Bit Locations (Rev C and later)

| | |
|---|---|
| 0xF | Bits 0-15, Axis 1 signal strength indicator (SSI) optical power for point 4; this value is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0x10 | Bits 0-5, Reference daisy chain delay value for use with the data age compensation algorithm.<br>Bits 6-15, Axis 2 measurement signal detector bias voltage (no signal) as measured during factory test. |
| 0x11 | Bits 0-7, Axis 2 signal strength indicator (SSI) A/D value for point 0; this value correspond to zero optical power; use this value with the SSI algorithm to determine the optical power of the measurement signal.<br>Bits 8-15, Axis 2 measurement channel delay value for use with the data age compensation algorithm. |
| 0x12 | Bits 0-15, Axis 2 signal strength indicator (SSI) A/D value for point 1; this value corresponds to the optical power at point 1; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0x13 | Bits 0-15, Axis 2 signal strength indicator (SSI) optical power for point 1; this is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0x14 | Bits 0-15, Axis 2 signal strength indicator (SSI) A/D value for point 2; this value corresponds to the optical power at point 2; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0x15 | Bits 0-15, Axis 2 signal strength indicator (SSI) optical power for point 2; this is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0x16 | Bits 0-15, Axis 2 signal strength indicator (SSI) A/D value for point 3; this value corresponds to the optical power at point 3; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0x17 | Bits 0-15, Axis 2 signal strength indicator (SSI) optical power for point 3; this value is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |
| 0x18 | Bits 0-15, Axis 2 signal strength indicator (SSI) A/D value for point 4; this value corresponds to the optical power at point 4; use this value with the SSI algorithm to determine the optical power of the measurement signal. |
| 0x19 | Bits 0-15, Axis 2 signal strength indicator (SSI) optical power for point 4; this value is the optical power input to the measurement receiver to obtain the A/D value located in previous memory address. |

**Table 3-15** EEPROM Data Register Bit Locations (Rev C and later) (continued)

### *ADC MUX Register*
### (Axis 1 only, 0x16 write only)

The ADC MUX Register is a write only register. The user selects the A/D converter channel by writing the channel number into bits 0-3 of this register. The power-on default value is 0. Writing to the ADC MUX Register restarts the analog-to-digital conversion process. The ADC ready bit in the Status Register indicates when the A/D converter result from the new mux value can be read.

### *Position Register*
### (Axis 1, 0x10, 0x12 read only) (Axis 2, 0x30, 0x32 read only)

An external sample (SCLK0) or a sample command (Command Register bit 9) operation latches the 36 bit value from the position accumulator into position register. The most significant 4 bits may be read from the High Nibbles Register, bits 0-3. A shifter can be configured using bits 12, to 15 in Control Register 1 so that any of the 36 position value bits can be latched into the least significant 32 bits of the position register. The value is a 2's complement number.

### *Sample Position Register*
### (Axis 1, 0x14, 0x16 read only) (Axis 2, 0x34, 0x36 read only)

An internal sample operation latches the current position accumulator value into the Sampled Position Register on each VME read of the sample position register.

The Sample Position Register is 36 bits, the most significant 4 bits may be read from the High Nibble Register, bits 4-7, after the Sample Position Register has been read. A shifter can be configured using bits 12 to 15 in Control Register 1 so that any of the 36 position value bits can be latched into the least significant 32 bits of the Sample Position Register. The value is a 2's complement number.

Read the upper 16 bits first when in the 16 bit mode.

### *Velocity Register*
### (Axis 1, 0x18, 0x1A read only) (Axis 2, 0x38, 0x3A read only)

The Velocity Register that contains the current stage velocity. The resolution of this register is dependent on the digital filter gains Kp and Kv. See "Velocity Circuit" in Chapter 4 for useful velocity resolution versus Kp and Kv gains.

The Velocity Register value is latched by the sample VME position command (Command Register bit 9), an external sample (SCLK0), or reading the Sample Position Register.

### *Time Register*
### (Axis 1, 0x1C, 0x1E read only) (Axis 2, 0x3C, 0x3E read only)

The Time Register is a read only register that contains the time at which the position sample was taken. One count equals 25 nanoseconds. Time is latched as a 32 bit positive value.

The Time Register value is latched by the sample VME position command (Command Register bit 9), an external sample (SCLK0), or reading the Sample Position Register.

### *P2 Interrupt Mask Register*
### (Axis 1, 0x1A write, 0x0C Mux 5 read)
### (Axis 2, 0x3A write, 0x2C Mux 5 read)

The P2 Interrupt Mask Register specifies the error conditions that generate P2 interface interrupts. The user writes a 1 into the bit locations corresponding to the desired interrupt generating errors. All interrupt mask bits are set to 0 (masked) during the power-on reset.

| *Bit* | *Action* | *Description* |
|---|---|---|
| 0 | Reference signal missing | Generates an interrupt when the reference signal is missing. |
| 1 | Reference PLL error | Generates an interrupt when the reference PLL is not locked. |
| 2 | Reference DLL error | Generates an interrupt when the reference DLL is not locked. |
| 3 | Measure signal missing | Generates an interrupt when the measurement signal is missing. |
| 4 | Measure signal dropout | Generates an interrupt when the measurement signal momentarily drops out. |
| 5 | Measure signal glitch | Generates an interrupt when the phase meter ASIC or data age compensator detects two or more edges on the measurement signal within a 40 MHz clock period. |
| 6 | Velocity error | Generates an interrupt when a velocity error is detected. |
| 7 | User velocity error | Generates an interrupt when the absolute value of the most significant 16 bits of the velocity exceeds the 16 bit value stored in the user excess velocity register. |
| 8 | Acceleration error | Generates an interrupt when an acceleration error occurs. |
| 9 | 36 bit position overflow | Generates an interrupt when the 36 bit position value overflows. |
| 10 | 32 bit position overflow | Generates an interrupt when the position value exceeds the user selected 32 bit window into the 36 bit position accumulator. On ASIC, revision B, this error may be inhibited by Control Register 2, bit 12. |

**Table 3-16** P2 Interrupt Mask Register Functions

## 3-6 P2 Bus Interface Operation

For 16 bit or 32 bit read selection, bit 9 of VME Control Register 1 must be set to 1.

### *P2 Bus Reset*

The Measurement Board uses the P2_RESET* signal to perform a position reset, quick position reset, time reset, and/or error latch reset. It does not perform a global reset like the VMEbus SYSRESET* signal or the VME reset axis command. Bits 3-6 in the VMEbus Control register 1 select which reset operations occur when the P2_RESET* signal is activated. The power-on default condition is that no reset operation is selected.

The error latch reset function resets the P2 interrupt latches which latch error conditions. When the error latch reset bit is set and the P2_RESET* signal is active, all P2 interrupt latches are cleared. If the error condition is still active, then the corresponding P2 interrupt latch is set again on the next clock. The user should clear the error condition before resetting the interrupt latches.

All error conditions can generate interrupts. The user writes a 1 into the masks bits 0-10 of the VMEbus P2 Interrupt Mask Control register determine which errors generate interrupts on the P2 interface. The power-on default condition is all mask bits set to no interrupts.

Error conditions are divided into fatal and non-fatal. P2 interrupt latches associated with fatal error conditions can be reset by writing to P2 interface offset address 0x01. The user velocity error is non-fatal. It's P2 interrupt latch can be reset by writing to address 0x02. The 32 bit overflow error is also non-fatal. It's P2 interrupt latch can be reset by writing to address 0x03. Hardware power-on reset and the VMEbus reset axis command resets all P2 interrupt latches.

| *P2 Interrupt Reset Write Address* | *P2 Interrupt Latches Reset* |
|---|---|
| 0x00 | Not used. |
| 0x01 | Reset all fatal error interrupt latches. (P2 status bits 21-27, 29, 30) |
| 0x02 | Reset user velocity interrupt latches. (P2 status bit 28) |
| 0x03 | Reset 32 bit overflow interrupt latches. (P2 status bit 31) |

**Table 3-17** P2 Interrupt Latch Reset Write Addresses

## 3-7 P2 Bus Signals

Refer to following table for a summary of the P2 signals. An asterisk(*) following a signal name indicates a true negative signal. P2 pin assignments are listed in Chapter 2.

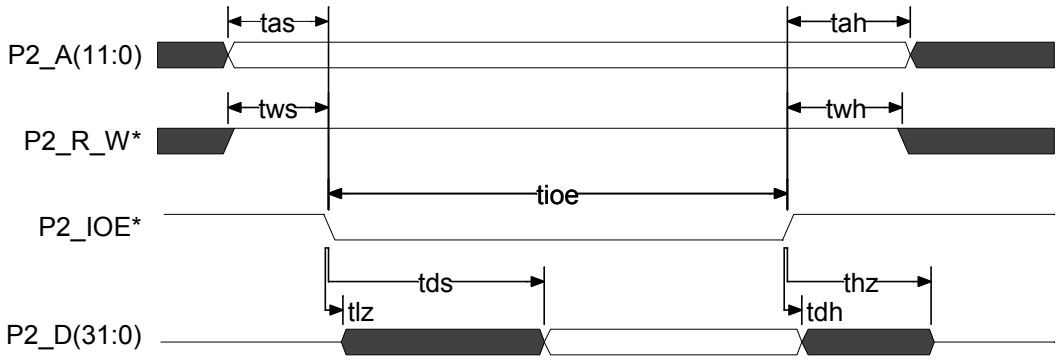
| *P2 pins* | *Signal* | *Description* |
|---|---|---|
| P2_D0 to P2_D31 | tri-state outputs | P2 data bus. The P2 data write cycle is a strobe function only, and does not require the data bus. For 32-bit data read, P2_D31 is the most significant bit and P2_D0 is the least significant bit. For 16-bit data read, P2_D31 is the most significant bit, P2_D16 is the least significant bit, and P2_D15 through P2_D0 are driven to an unspecified state. 16 or 32 bit data transfer is defined by bit 9 in VMEbus Control Register 1. |
| P2_A0 to P2_A11 | inputs | The address bus for the P2 interface. A11 is the most significant bit and A0 is the least significant bit. The base address is set by SW5, switches 1-8. |
| P2_R/W* | input | Read/Write, high for read, low for write. |
| P2_RESET* | input | P2 reset signal. The action of this signal is defined by bits in VME Control Register 1. |
| P2_INT0* to P2_INT3* | outputs | P2 interrupt lines. They are jumper selectable for open-collector active-low, totem-pole active low, or totem-pole active high outputs. The open collector active-low choice is preferred since it allows multiple boards to share interrupts, and a board may be missing without causing an interrupt. For use with the open-collector driver, this line should have a 330Ω pull-up resistor on the backplane or on the bus master. |
| P2_SCLK0 | input/ output | Sample Clock 0, used to sample multiple axes at the same instant. This signal is driven by the last board in the reference daisy chain and received by all other boards. This signal is not intended to be driven by the user. SCLK0 can also be programmed to drive the bus with a periodic signal. This is used to sample data on several boards while minimizing the data age uncertainty between the samples. |
| P2_SCLK1 | input | Sample Clock 1. This signal is driven by the user into the last board in the reference daisy chain when an externally generated sample signal is required. The input is synchronized to the 20 MHz reference clock, then output to all boards as SCLK0. The polarity and enable is controlled by SW5, positions 9 and 10; see Table 2-6. By changing jumper positions of JN6, SCLK0 and SCLK1 may be swapped. |
| P2_IOE* | input | I/O Enable, active-low during a read or write cycle. The address lines and the P2_R/W* signals must be stable while this line is low, as shown in the timing diagrams. |

**Table 3-18** P2 Bus Signal Descriptions

# 3-8 P2 Timing Diagrams

## *P2 Read Cycle Timing*

The timing for the read cycle is shown below. This timing restricts the maximum asynchronous data rate to approximately 7 MHz.

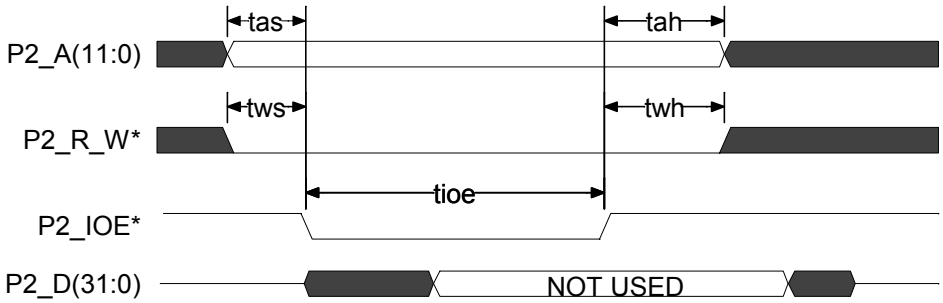



| *Symbol* | *Parameter* | *Min* | *Max* | *Units* |
|---|---|---|---|---|
| tas | Address Setup time | 10 | | ns |
| tws | Write Setup time | 10 | | ns |
| tioe | IOE pulse duration | 110 | | ns |
| tah | Address Hold time | 10 | | ns |
| twh | Write Hold time | 10 | | ns |
| tlz | IOE low to active output | 0 | | ns |
| thz | IOE high to high Z output | | 20 | ns |
| tds | Data setup from IOE low | | 60 | ns |
| tdh | Data hold from IOE high | 0 | | ns |

**Figure 3-3** P2 Bus Read Cycle

For faster operation, or for synchronous operation, data can be latched synchronously by the SCLK0 signal provided by the same ZMI board at rates up to 10 MHz. Contact Zygo for an example of user hardware for this application or for additional information.

### *P2 Write Cycle Timing*




| *Symbol* | *Parameter* | *Min* | *Max* | *Units* |
|---|---|---|---|---|
| tas | Address Setup time | 10 | | ns |
| tws | Write Setup time | 10 | | ns |
| tioe | IOE pulse duration | 110 | | ns |
| tah | Address Hold time | 10 | | ns |
| twh | Write Hold time | 10 | | ns |

**Figure 3-4** P2 Bus Write Cycle

## 3-9 P2 Bus Registers

### *Register Address Map*

The table below shows the offset address for the P2 registers.

| *Axis Address (hex)* | | *16 Bit Data Path* | *32 Bit Data Path* |
|---|---|---|---|
| *2* | *1* | *(D31-D16)* | *(D31-D0)* |
| F | 7 | Time data (LSB) | Invalid data |
| E | 6 | Time data (MSB) | Time data |
| D | 5 | Velocity data (LSB) | Invalid data |
| C | 4 | Velocity data (MSB) | Velocity data |
| B | 3 | Position data (LSB) | Invalid data |
| A | 2 | Position data (MSB) | Position data |
| 9 | 1 | Status and High Nibble bits (LSB) | Invalid data |
| 8 | 0 | Status and Error bits (MSB) | Status, Error, and High Nibble bits |

**Table 3-19** P2 Bus Interface Memory Map

The P2 position, time, and velocity values are latched by the SCLK0 input if P2 latch mode (Control Register 1, bit 8) is set to 0. The position, time, and velocity values are latched by reading position data (MSB first in 16-bit mode) if P2 latch mode is set to 1.

## *Status, Error, and High Nibble P2 Interface Register*

This register contains the status bits, error bits, and the 4 high order position data bits. The table below lists the bit positions of these signals in the register. See "Error Detection and Status Reporting" section later in this chapter for details on bits 21-31.

| *Bit* | *Signal (LSB)* | *Bit* | *Signal (MSB)* |
|---|---|---|---|
| 0 | 1 (not used) | 16 | Reference signal present |
| 1 | 1 (not used) | 17 | Reference PLL locked |
| 2 | 1 (not used) | 18 | Reference DLL locked |
| 3 | 1 (not used) | 19 | Measurement signal present |
| 4 | 1 (not used) | 20 | Position reset complete |
| 5 | 1 (not used) | 21 | Reference signal missing |
| 6 | 1 (not used) | 22 | Reference PLL error |
| 7 | 1 (not used) | 23 | Reference DLL error |
| 8 | 1 (not used) | 24 | Measure signal missing |
| 9 | 1 (not used) | 25 | Measure signal dropout |
| 10 | 1 (not used) | 26 | Measure signal glitch |
| 11 | User bit | 27 | Velocity error |
| 12 | Position data bit 33 | 28 | User velocity error |
| 13 | Position data bit 34 | 29 | Acceleration error |
| 14 | Position data bit 35 | 30 | 36 bit position overflow |
| 15 | Position data bit 36 | 31 | 32 bit position overflow |

**Table 3-20** Status, Error, and High Nibble P2 Interface Register

The high nibble bits are latched at the same time as the P2 Position Register, and should be read after the position is read. The error bits 31-21, have the same meaning as the corresponding errors in the VME Error Status Register, bits 10-0. The P2 Error Register is set and reset separately from the VME Error Status Register.

The status bits 20-16 have the same meaning as the corresponding status in the VME Status Register, bits 4-0. The user bit shows the state of the user P2 bit (VME Control Register 1, bit 2).

# 3-10 Data Age

## *Definition/Explanation of Data Age*

To accurately control the precision motion it is necessary to provide not only position data but also time data; when the measured object is at that exact location. Data age is defined as the difference in the time between when the user object is measured and when the user control system gets the position information. Data age uncertainty is defined as the maximum variation in the data age in a multi-axis system, due primarily to process variations in the electronics.

On a single axis measurement, the data age is approximately 335 ns. The data age must be known so that servo loops using the ZMI-2002 as a sensor can be properly compensated. The exact value of data age for a single axis measurement is usually not important, as long as it is constant.

On a multiple axis measurement, data age differences among axes must be minimized. The system is intended to measure the position of an object moving as fast as 2 m/s with a resolution of λ/2048 (0.3 nm). At this velocity, a time delay in the measurement signal path of 1ns corresponds to a position error of 2 nm. For some applications such as angle measurements, matching between the two measurement axes is important.

Multiple boards are synchronized in two ways. The phase meters are synchronized by the 20 MHz reference passed through the reference daisy chain. The measurement output is synchronized by the SCLK0 signal on the P2 bus. SCLK0 must be driven by the last board in the daisy chain to insure proper operation of all boards.

Data age compensation is achieved through internal Measurement Board circuitry which adjusts the data age for a position value. The resultant compensated data age is reduced to the lowest possible level, and is transparent to the motion control system.

In the ZMI-2002, data age is defined as the time from a reference signal edge to when the corresponding position value is latched by the SCLK0 sample clock. In a multi-axis system, the data age of each axis is with respect to the first axis in the reference signal daisy chain.

| *Axes* | *Board* | *Data Age Range (ns)* | *Compensated Data Age Uncertainty Worst Case (ns)* |
|---|---|---|---|
| 1-2 | 1 | ±12.5 | ±0.5 |
| 3-4 | 2 | -9.5, +15.5 | ±1.0 |
| 5-6 | 3 | -6.9, +19.0 | ±1.2 |
| 7-8 | 4 | -4.4, +22.6 | ±1.4 |
| 9-10 | 5 | -1.8, +26.1 | ±1.6 |
| 11-12 | 6 | -0.7, +29.6 | ±1.8 |

**Table 3-21** Position Data Age Uncertainty for Multi-Axis Systems

The uncompensated data age of the two axes within any one measurement board is less than ±12.5 ns. The compensated data age of the two axes within any one measurement board is ±0.5 ns.

## Data Age Compensation

Some high precision, high speed applications require the user to minimize data age uncertainty. To determine if data age compensation should be enabled, the user should calculate if data age uncertainty exceeds the error budget. This error is calculated by V*T = error. Typical data age uncertainty is approximately 10 nanoseconds for the ZMI-2002.

## Compensation Algorithm

The ZMI-2002 data age uncertainty can be reduced by adding a fixed value to the phase measurement. The user reads factory stored data from the onboard EEPROM, then computes a compensation value using the algorithm below. The user then writes this value to the Data Age Adjust Register.

The data age adjust value has a range of ± 24.9 ns with a resolution of 97.7 psec. The power-on default value is 0 nsec. The read and write locations are different. The user can read back these bits by reading one of the muxed register locations.

*Data age uncertainty compensation value algorithm*

1. Read the measurement channel delays, M, for each board from the EEPROM on each board.
2. Read the reference daisy chain delay, D, for each board from the EEPROM on each board.
3. Compute the total delay for each board.
   For board 1: total delay = M1
   For board 2: total delay = M2 - D2
   For board 3: total delay = M3 - D2 - D3
4. Determine the minimum and maximum total delay from all computed values.
5. Compute the mean of the minimum and maximum values.
6. Subtract the total delay of each board from the mean.
7. Load the integer result into the Data Age Adjust Register.

## Compensation Verification

The data age compensation may be directly verified using the Phase Meter Diagnostic Register. This requires a program that will read the 9 bit phase value a number of times (typically 100), compute an average phase, and convert it to time (1 LSB = 97.7 ns). See the register description for details on how to read this register. Note that special methods must be used for this average, since the data represents an angle (for example, the average of 6 and 510 is 2, not 258).

1. Setup the system with a null interferometer.
2. Initialize all axes, including the data age registers.
3. Connect the fiber optic cable for the axis to be measured to the null interferometer.
4. Measure the phase using the test program and the Phase Meter Diagnostic Register.

To verify the board specifications and compensation algorithm, repeat steps 3 and 4 for each axis, using the same fiber optic cable connected to each board in turn. Compare the results for each axis. The differences between axes should be less than the maximum values listed in Table 3-21.

To verify the system level data age compensation, repeat steps 3 and 4 using the fiber optic cables that will be used in the application, connected to the null interferometer in turn. Compare the results for each axis. The results of this test will depend on the differences in the lengths of the fiber optics.

## 3-11 Digital Filtering

### *Purpose of the Digital Filter*

A digital filter circuit on the Measurement Board is designed to remove noise from the measurement data. The Measurement Board uses a second order digital filter, with two programmable gains, Kp and Kv, to permit a wide range of low pass filter cutoff frequencies, from 15 kHz to 3.8 MHz.

A functional description of the digital filter is in Chapter 4.

### *Filter Equations*

The equations below show the transfer function for the digital filter. The next section provides the filter performance versus all possible gain combinations.

$z(f) = e^{-j2\pi fTc}$ $\quad Tc = 40\ MHz \quad Xp = 2^{Kp} \quad Xv = 2^{Kv}$

**Equation 1** Position Transfer Function of the Digital Filter:

$$\frac{POut}{PIn} = \left[\left(X_p - X_v\right)\cdot z(f) - X_p\right]\cdot\frac{z(f)^3}{\left[\left(X_p - X_v\right)\cdot z(f)^4 - z(f)^3\cdot X_p - z(f)^2 + 2\cdot z(f) - 1\right]}$$

**Equation 2** Velocity Transfer Function of the Digital Filter:

$$\frac{VOut}{PIn} = (1 - z(f))\cdot z(f)^2\cdot\frac{X_v}{\left(-X_p + X_v\right)\cdot z(f)^4 + z(f)^3\cdot X_p + z(f)^2 - 2\cdot z(f) + 1}$$

## *Selecting Kv and Kp Values*

The user should calculate the desired feedback bandwidth for their particular application. The proper Kp and Kv values should be selected according to the required bandwidth and desired settling times shown in the filter performance tables.

For a step and repeat system, which has a fast settling requirements, appropriate filter values might be Kp = -8 and Kv = -18. This would provide a bandwidth of 31 kHz while providing a settling time to 1 LSB of 40 µsec.

For a scanning operation required a larger bandwidth, a possible combination might be Kp = -7 and Kv = -16. This provides a -3 dB bandwidth of 63 kHz.

## *Filter Performance Tables*

The following tables provide digital filter performance information for all Kp and Kv gain combinations. The first row, labeled Kp, contains actual Kp gain values. The user programs the Kp register with a number from the cells under the Kp values. The first column, labeled Kv, contains the actual Kv gain values. The user programs the Kp Register with a number from the cells to the left of the Kv values. X = filter unstable. Do not use these gain combinations.

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | 3795 | X | X | X | X | X | X | X |
| -8 | 1 | 3869 | 1462 | 830 | X | X | X | X | X |
| -10 | 2 | 3891 | 1314 | 585 | 387 | X | X | X | X |
| -12 | 3 | 3896 | 1273 | 506 | 267 | 187 | X | X | X |
| -14 | 4 | 3898 | 1262 | 485 | 229 | 128 | 92 | X | X |
| -16 | 5 | 3898 | 1260 | 480 | 219 | 110 | 63 | 46 | X |
| -18 | 6 | 3898 | 1259 | 479 | 217 | 105 | 54 | 31 | 23 |
| -20 | 7 | 3898 | 1259 | 478 | 216 | 104 | 51 | 27 | 15 |

**Table 3-22A** -3dB Bandwidth of Digital Filter (kHz)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | 3.4 | X | X | X | X | X | X | X |
| -8 | 1 | 1.4 | 1.7 | 4.7 | X | X | X | X | X |
| -10 | 2 | 1.1 | 0.5 | 1.4 | 3.9 | X | X | X | X |
| -12 | 3 | 1.0 | 0.1 | 0.4 | 1.3 | 3.6 | X | X | X |
| -14 | 4 | 1.0 | 0.0 | 0.1 | .4 | 1.3 | 3.5 | X | X |
| -16 | 5 | 1.0 | 0.0 | 0.0 | .1 | .4 | 1.3 | 3.4 | X |
| -18 | 6 | 1.0 | 0.0 | 0.0 | .0 | .1 | .4 | 1.3 | 3.4 |
| -20 | 7 | 1.0 | 0.0 | 0.0 | .0 | .0 | .1 | .4 | 1.3 |

**Table 3-22B** Gain Peaking of Digital Filter (dB)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | <1 | X | X | X | X | X | X | X |
| -8 | 1 | <1 | <1 | <1 | X | X | X | X | X |
| -10 | 2 | 9 | 3 | 2 | 1 | X | X | X | X |
| -12 | 3 | 78 | 31 | 14 | 6 | 7 | X | X | X |
| -14 | 4 | 450 | 200 | 93 | 44 | 17 | 18 | X | X |
| -16 | 5 | 2400 | 1100 | 520 | 250 | 120 | 44 | 57 | X |
| -18 | 6 | 12000 | 5400 | 2700 | 1300 | 640 | 300 | 110 | 160 |
| -20 | 7 | 48000 | 24000 | 13000 | 6400 | 3200 | 1600 | 750 | 260 |

**Table 3-22C** Settling Time to 1 LSB with 100G Ramp Acceleration (μsec)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | <1 | X | X | X | X | X | X | X |
| -8 | 1 | <1 | <1 | <1 | X | X | X | X | X |
| -10 | 2 | 2 | 2 | 2 | 2 | X | X | X | X |
| -12 | 3 | 9 | 8 | 8 | 8 | 8 | X | X | X |
| -14 | 4 | 35 | 34 | 33 | 33 | 33 | 33 | X | X |
| -16 | 5 | 140 | 140 | 130 | 130 | 130 | 130 | 130 | X |
| -18 | 6 | 430 | 510 | 530 | 520 | 520 | 520 | 520 | 520 |
| -20 | 7 | 650 | 1100 | 1600 | 2000 | 2100 | 2100 | 2100 | 2100 |

**Table 3-22D** Overshoot with 100G Ramp Acceleration (LSB)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | <0.5 | X | X | X | X | X | X | X |
| -8 | 1 | 0.5 | 0.5 | 0.5 | X | X | X | X | X |
| -10 | 2 | 2.1 | 2.0 | 2.1 | 2.1 | X | X | X | X |
| -12 | 3 | 8.1 | 8.1 | 8.1 | 8.1 | 8.1 | X | X | X |
| -14 | 4 | 32 | 32 | 32 | 32 | 33 | 33 | X | X |
| -16 | 5 | 130 | 130 | 130 | 130 | 130 | 130 | 130 | X |
| -18 | 6 | 320 | 440 | 510 | 520 | 520 | 520 | 520 | 520 |
| -20 | 7 | 450 | 800 | 1300 | 1800 | 2000 | 2100 | 2100 | 2100 |

**Table 3-22E** Following Error with 100G Ramp Acceleration (LSB)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | <1 | X | X | X | X | X | X | X |
| -8 | 1 | <1 | <1 | <1 | X | X | X | X | X |
| -10 | 2 | <1 | <1 | <1 | <1 | X | X | X | X |
| -12 | 3 | <1 | <1 | <1 | <1 | <1 | X | X | X |
| -14 | 4 | <1 | <1 | <1 | <1 | <1 | <1 | X | X |
| -16 | 5 | 330 | 100 | 42 | 16 | 8 | 6 | 5 | X |
| -18 | 6 | 3600 | 1600 | 750 | 360 | 175 | 84 | 40 | 25 |
| -20 | 7 | 22000 | 12000 | 5400 | 2700 | 1300 | 640 | 310 | 130 |

**Table 3-22F** Settling Time to 1 LSB with 1G Ramp Acceleration (μsec)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | <1 | X | X | X | X | X | X | X |
| -8 | 1 | <1 | <1 | <1 | X | X | X | X | X |
| -10 | 2 | <1 | <1 | <1 | <1 | X | X | X | X |
| -12 | 3 | <1 | <1 | <1 | <1 | <1 | X | X | X |
| -14 | 4 | <1 | <1 | <1 | <1 | <1 | <1 | X | X |
| -16 | 5 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | X |
| -18 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| -20 | 7 | 23 | 22 | 22 | 22 | 21 | 21 | 21 | 21 |

**Table 3-22G** Overshoot with 1G Ramp Acceleration (LSB)

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | <0.5 | X | X | X | X | X | X | X |
| -8 | 1 | <0.5 | <0.5 | <0.5 | X | X | X | X | X |
| -10 | 2 | <0.5 | <0.5 | <0.5 | <0.5 | X | X | X | X |
| -12 | 3 | <0.5 | <0.5 | <0.5 | <0.5 | <0.5 | X | X | X |
| -14 | 4 | <0.5 | <0.5 | <0.5 | <0.5 | <0.5 | <0.5 | X | X |
| -16 | 5 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | X |
| -18 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| -20 | 7 | 19 | 21 | 21 | 21 | 21 | 21 | 21 | 21 |

**Table 3-22H** Following Error with 1G Ramp Acceleration (LSB)

## 3-12 Error Detection and Status Reporting

The Measurement Board interface ASIC detects and reports the error conditions listed below. Error conditions that corrupt the position data are marked as fatal errors.

| *Error Condition* | *Fatal Error* | *Description* |
|---|---|---|
| Reference signal missing | yes | Indicates that the reference signal is missing. |
| Reference PLL error | yes | Indicates that the reference PLL is not locked. |
| Reference DLL error | yes | Indicates that the reference DLL is not locked. |
| Measure signal missing | yes | Indicates that the measurement signal is missing. |
| Measure signal dropout | yes | Indicates that the measurement signal momentarily dropped out. (period  250 ns) |
| Measure signal glitch | yes | Indicates that the phase meter ASIC or the data age adjust circuitry detected two or more edges on the measurement signal within a 40 MHz clock period. |
| Velocity error | yes | Indicates that a velocity error was detected. Normally, this means that the velocity exceeded 2.1 m/sec (measurement frequency <6.67 MHz or >33.6 MHz). If the disable excess velocity bit (Control Register 2, bit 15) is set, the high frequency limit is ignored. |
| User velocity error | no | Indicates that the absolute value of the most significant 16 bits of the velocity exceed the 16 bit value stored in the user excess velocity register. This bit can be reset with the reset user velocity error bit (Command Register, bit 7). |
| Acceleration error | yes | Indicates that an acceleration error has occurred. This error indicates an overflow within the digital filter. With any of the stable Kp and Kv values listed in the "Digital Filtering" section later in this chapter, the limit is well above 100g. |
| 36 bit position overflow | yes | Indicates that the 36 bit position value has overflowed. |
| 32 bit position overflow | no | Indicates that the position value exceeded the user selected 32 bit window into the 36 bit position accumulator. This bit can be reset with the reset 32 bit position overflow bit (Command Register, bit 10). With revision A ASIC, this error may occur in 36 bit mode unless the bit window (Control Register, bits 12-14) is set to 100. With revision B ASIC, this error is inhibited unless Control Register 2, bit 12 is 1. |

**Table 3-23** Error Conditions

The error conditions are subdivided into fatal and nonfatal error. Fatal errors are conditions which corrupt the position data and intermediate values in the digital filter. For example, if the 36 bit position value overflows, then the data fed back into the filter will be unknown, thus the output of the filter will also be unknown. A measurement board must be reset if a fatal error occurs. Nonfatal errors do not corrupt the position data. The user can reset nonfatal error once the condition stops generating an error.

The structure of the VMEbus and P2 Error Registers is shown in the following figure.

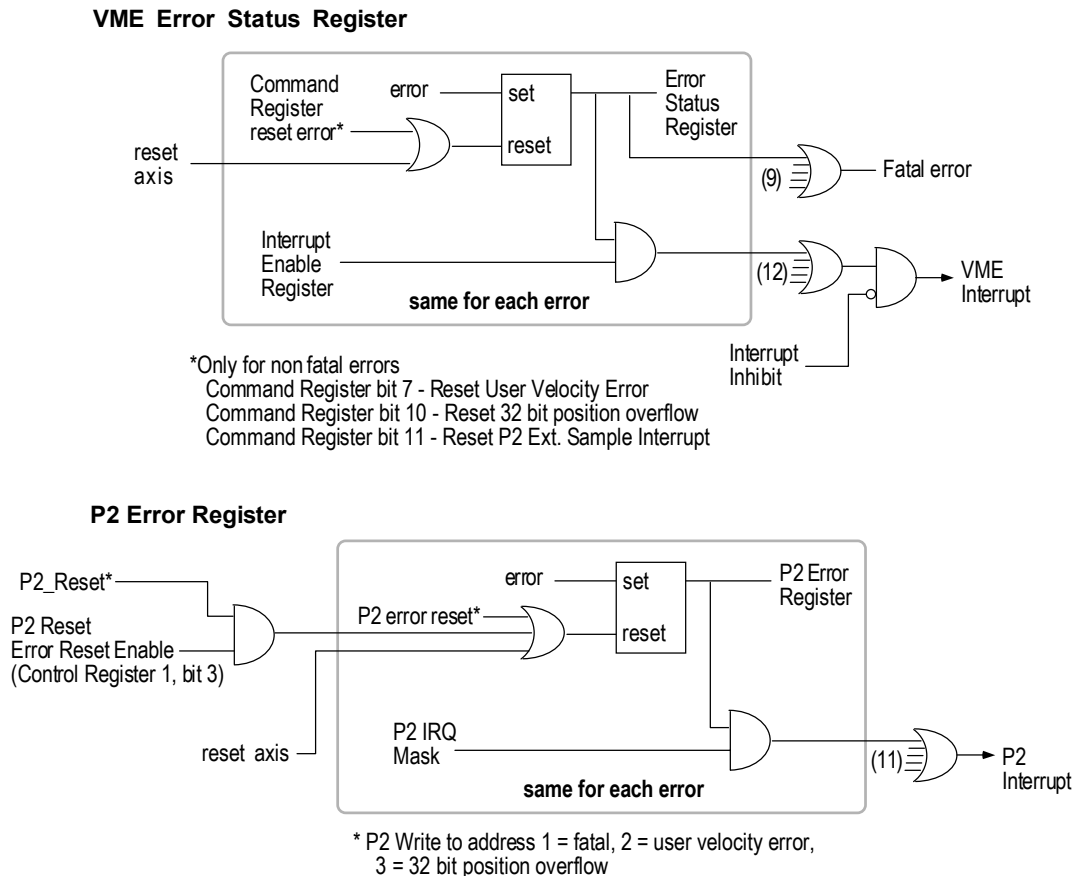



**Figure 3-5** Error Registers

The interface ASIC also reports the status conditions listed in the following table.

| *Status Condition* | *Description* |
|---|---|
| Reference signal present | Indicates that the board is receiving a valid reference signal. |
| Reference PLL locked | Indicates that reference phase locked-loop has locked on to the incoming reference signal. |
| Reference DLL locked | Indicates that the delay locked-loop has locked and that the tap-to-tap delay is controlled. |
| Measurement signal present | Indicates that the board is receiving a valid measurement signal. |
| Position reset complete | Indicates that the reset position command has been completed. |
| External sample flag | Indicates that an external sample command has been received. |

**Table 3-24** Status Conditions

These errors are displayed on the front panel LED's and can be read through the VMEbus and P2 interfaces. The interrupt output on the P2 connector becomes active when an error occurs and the corresponding bit in the P2 Interrupt Mask Register is set. This signal can generate an interrupt to an P2 Bus compatible CPU board connected to the Measurement Board.

Error interrupt latches are cleared by the power-on reset and by writing to the reset bit(s) in a command register. The latches will be set again on the next 40 MHz clock if the error condition remains.

## 3-13 Signal Strength Indicator Algorithm

The measurement signal receiver and signal strength indicator circuit outputs are non-linear and can have a wide variation due to component tolerances. Thus, the non-volatile memory (EEPROM Data register) on each board has been factory programmed with calibration data. This calibration data can be used to determine the optical power of the measurement signal relatively accurately (±10%).

Five data points are stored in the EEPROM Data register, these correspond to a piece-wise linear approximation of the optical power input versus A/D value transfer function.

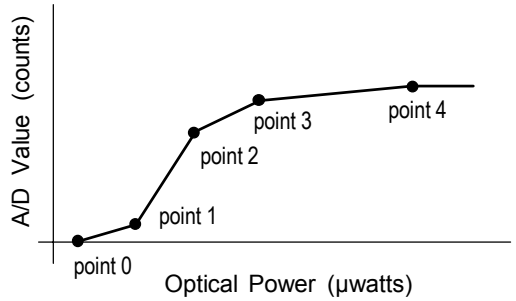



**Figure 3-6** Typical Optical Power Graph

This data may be used to calculate four linear equations. The user must then determine which linear segment to use to convert each A/D value into microwatts. Point 0 is for an optical power input of zero. Point 4 indicates the first saturation point in the transfer function.

### *Calculating the Optical Power*

1. Read the five calibration points for each measurement axis from the non-volatile memory (EEPROM Data register).
2. Compute the slope, m, and intercept, y, for the linear equation $y = mx + b$. Where x is the A/D value in counts and y is the corresponding optical power in microwatts.
3. As required by the application, read the optical power from the A/D.
4. Determine which linear equation to use given the A/D value range.
5. Compute the optical power in microwatts.

# *Chapter 4* Functional Description

### *In This Chapter*


4-1 ZMI System Overview
4-2 Measurement Board Operation
4-3 Phase Meter ASIC
4-4 Interface ASIC
- Data Age Compensator
- ΔPosition Calculator
- Position Interpolator
- Digital Filter
- Position Accumulator
- Time Accumulator
- Velocity Circuit


## 4-1 ZMI System Overview

A typical single axis ZMI system is shown in Figure 4-1. The main components are: a laser head, an interferometer, and a ZMI-2002 Measurement Board.

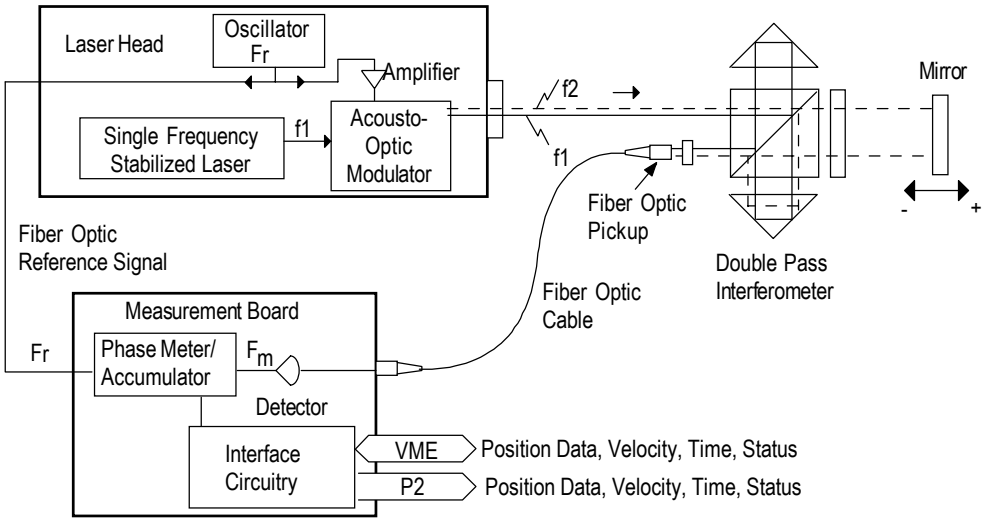



**Figure 4-1** ZMI System Block Diagram

The laser head consists of stabilized laser, an acousto-optic modulator and a 20 MHz oscillator. The laser head provides a beam with two orthogonal linear polarizations having different frequencies. One frequency, f1, is vertically polarized and is 20 MHz higher in frequency than f2. The second frequency, f2, is horizontally polarized. The laser head outputs an optical reference signal equal to the difference of f1 - f2.

The interferometer can be a single pass, double pass, or four pass design. (Resolution requirements determine the interferometric configuration.) A double pass interferometer consists of a polarizing beamsplitter, two retroreflectors, a quarter waveplate and a mirror. The polarizing beamsplitter divides the laser beam into its two frequency components and directs one component to a stationary retroreflector and the other to a moving mirror. Optical path changes in the interferometer phase modulate the difference frequency f1 - f2. The optical measurement signal is directed to the Measurement Board by a fiber optic cable.

At the ZMI-2002 Measurement Board, a photoelectric detector converts the optical signal from the interferometer into an electrical measurement signal ($F_m$) and the optical reference signal from the laser head into an electrical reference signal ($F_r$). $F_m$ has a phase proportional to the phase difference of f1 and f2. This interference signal phase change is determined by comparing the phase of the interference signal to the phase of the reference signal. Phase changes of $F_m$ relative to $F_r$ are accumulated in a register to indicate position change. A digital filter smoothes and accumulates each incremented position value.

## 4-2 Measurement Board Operation

The Measurement Board is a register based VMEbus slave card. It converts the optical phase information of the interferometer measurement and reference signals to a 36 bit (or 32 bit) 2's complement position value. The measurement data is uncompensated and in units of wavelength/2*N*512 , where N is the number of passes in the interferometer.

The position data is accumulated by using two Application Specific Integrated Circuits (ASIC) on the Measurement Board. The first ASIC contains the phase meter portion of the design. The interface ASIC provides the position interpolation, digital filtering, P2 interfacing, VMEbus interfacing, and error detection/reporting. The Measurement Board block diagram is shown in Figure 4-2. There are two interfaces for reading position data. One through the VME data transfer bus and the other through the P2 connector.

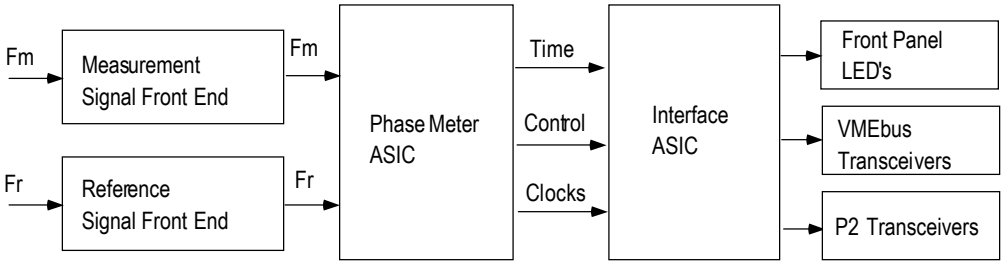



**Figure 4-2** Measurement Board Block Diagram

## 4-3 Phase Meter ASIC

The phase meter ASIC is custom designed to measure position change at high resolution and high velocities with very small error. It converts the analog phase into a digital value. A block diagram of the phase meter ASIC is shown in Figure 4-3.

The phase meter ASIC measures the time from the rising edge of the measurement signal relative to the previous edge of the 40 MHz reference clock. This measurement is performed using a tapped delay line interpolator. The delay line includes circuitry to control the tap-to-tap delay.

The ASIC includes a PLL which multiplies the 20 MHz clock by 64 creating a 1280 MHz clock. This clock is required to convert the analog signal to phase at 20 MHz over the full Doppler shift frequency range. The ASIC also outputs control, error, and clock signals used by the position interpolator and digital filter.

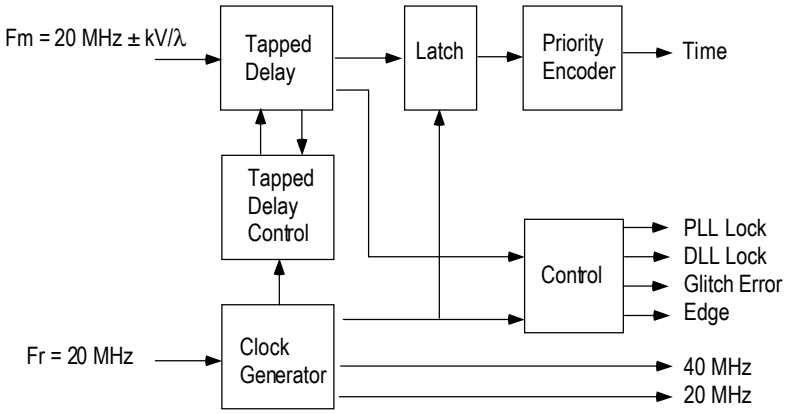



**Figure 4-3** Phase Meter ASIC Block Diagram

## 4-4 Interface ASIC

The interface ASIC performs functions in eight basic areas: data age compensation, Δposition calculation, position interpolation, digital filtering, position and time accumulation, VMEbus interface, P2 interface, and error detection/reporting. A block diagram of the interface ASIC is shown in Figure 4-4

Most of the above mentioned interface ASIC functions are described in the sections that follow. The VMEbus interface and P2 interface are described in Chapter 1. Error detection and reporting is described in Chapter 3.

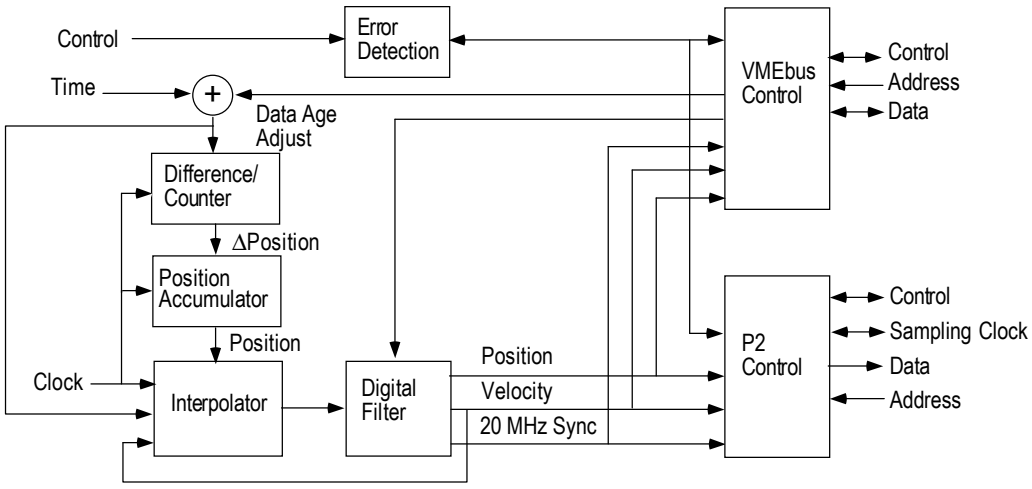



**Figure 4-4** Interface ASIC Block Diagram

## *Data Age Compensator*

The phase meter ASIC measures the instantaneous phase between the reference and measurement signals by measuring the time between the rising edge of the reference signal and the rising edge of the measure signal. This time value is output to the interface ASIC. The interface ASIC uses these values and an internal counter to compute Δposition. The Δposition values are accumulated to provide a position value. It then interpolates and filters position data and outputs the resulting position values.

The data age compensation circuit adds a correction value to the time data inside the interface ASIC before Δposition is calculated. It is possible to eliminate the data age uncertainty due to process variations and the board-to-board reference daisy chain by measuring the data age of specific circuits on each Measurement Board. This data is stored in non-volatile memory on each board. The user reads this data and computes a correction value using a Zygo supplied algorithm. The correction value is written into the Measurement Board Data Age Adjust Register.

Information on adjusting data age can be found in Chapter 3.

## *ΔPosition Calculator*

The Δposition calculation circuit uses the compensated time value for the lower order bits in the phase value. It uses the 40 MHz clock from the phase meter ASIC and a time interval counter in the interface ASIC to generate the higher order bits. Two consecutive phase values are subtracted from each other to produce a Δposition value.

## Position Accumulator

The position accumulator sums Δposition values to produce a position value. This position value represents the position at the time when the measurement edge occurred.

Bit 14 in Control Register 2 can be used to change the direction sense of the position value. A position reset must be executed after changing the direction sense because changing this function corrupts the data in the digital filter. The position accumulator value is stored as a 2's complement value.

## Position Interpolator

The position interpolator receives position from the position accumulator. The position value is adjusted to compensate for the time difference between when the edge actually happened and when the next edge of the 40 MHz clock sampled it. A block diagram of the position interpolator is shown in Figure 4-5.

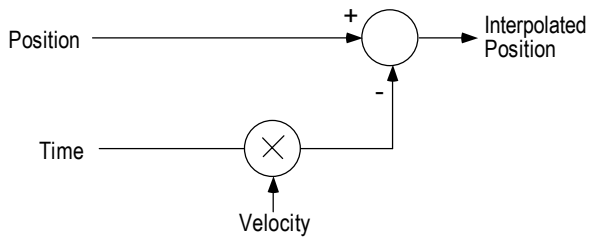



**Figure 4-5** Position Interpolator Block Diagram

To eliminate data age uncertainty due to the Doppler shift in the measurement signal, the Measurement Boards interpolate position values at a constant rate from past position data. This provides the system with position data at a fixed sampling rate with very low data age uncertainty. Also, all Measurement Board clocks are synchronized with each other to reduce the board-to-board data age to the lowest possible value.

## Digital Filter

The digital filter removes noise from the measurement data. A digital filter provides greater performance over an analog front end filter and PLL. Digital filters are not susceptible to induced noise and do not vary with component tolerance or temperature. A block diagram of the digital filter is shown in Figure 4-6.

The Measurement Board uses a programmable second order digital filter. The second order digital filter smoothes the output from the interpolator. This design includes two additional latches to allow sufficient time for adder propagation delay. The two programmable gains, Kp and Kv, permit a wide range of low pass filter cutoff frequencies, from 15 kHz to 3.8 MHz.

Information on using the digital filter can be found in Chapter 3.

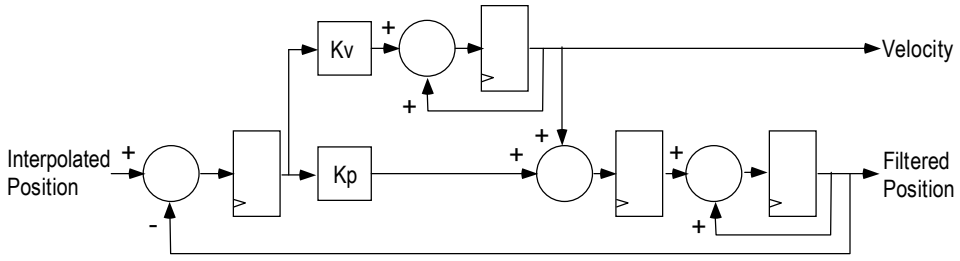



**Figure 4-6** Digital Filter Block Diagram

## *Position Formatter*

The position formatter formats the position output from the digital filter. The resultant position value is a 36 bit number. The most significant 4 bits of the position are always output to the High Nibbles Register. The entire 36 bit position value is, however, input to a shifter. The shifter fits any 32 bits of the 36 position accumulator bits into the least significant 32 bits of the position registers. This permits a host computer to read a single 32 bit value from the measurement board, while accessing any of the 36 position bits.

The 36 bit position accumulator overflow error is fatal because the data fed back to the digital filter input after an overflow occurs is unknown. The 32 bit position window overflow error indicates that the position value has exceed the user selected 32 bits. This is not a fatal error unless it is a result of a 36 bit position overflow.

A block diagram of the position and offset registers is shown in Figure 4-7.

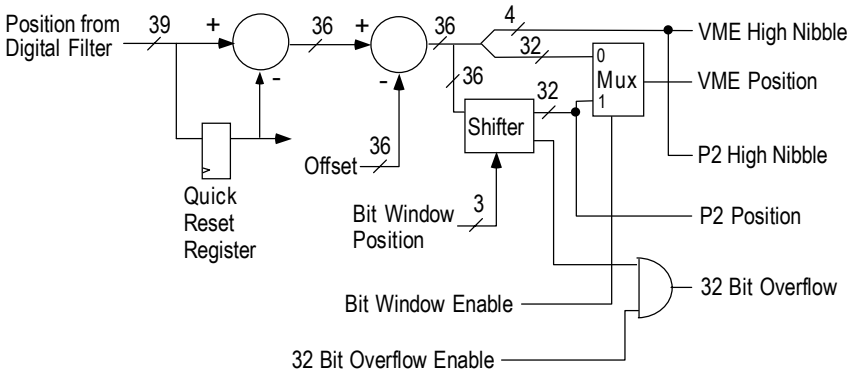



**Figure 4-7** Position and Offset Registers

### *Time Accumulator*

The time accumulator accumulates 25 nanosecond clock ticks. The time accumulator value is latched into the time register each time a position accumulator value is latched into a position register. The value is stored as a 32 bit positive integer.

### *Velocity Circuit*

The velocity is calculated by the digital filter. It outputs a 32 bit 2's complement value. The least significant bit in the velocity register has a nominal resolution of 0.0029467 µm/sec for a plane mirror interferometer and is independent of the digital filter gains.

The useful resolution of the velocity register, however, is a function of the digital filter gains because they are used in calculating the velocity. When Kp and Kv are programmed to -9 and -20 respectively, the digital filter has a bandwidth of 15 kHz. This relatively high level of filtering produces a high resolution velocity calculation. When Kp and Kv are programmed to -2 and -6 respectively, the digital filter bandwidth is 3.8 MHz. This relatively low level of filtering produces a low resolution velocity calculation. Thus, while the resolution of the velocity register has not changed, the useful resolution of the value read from the register has changed.

Table 4-1 indicates the number of significant bits in the velocity register as a function of Kp and Kv. The negative numbers are the actual gain values. The user programs 0 to 7 into the Kp and Kv registers to get actual gain values. Boxes marked with an X indicate unstable filter combinations.

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | 17 | X | X | X | X | X | X | X |
| -8 | 1 | 19 | 18 | 18 | X | X | X | X | X |
| -10 | 2 | 21 | 21 | 20 | 20 | X | X | X | X |
| -12 | 3 | 17 | 20 | 23 | 22 | 22 | X | X | X |
| -14 | 4 | 18 | 18 | 19 | 20 | 24 | 23 | X | X |
| -16 | 5 | 20 | 19 | 20 | 20 | 21 | 25 | 23 | X |
| -18 | 6 | 22 | 21 | 21 | 21 | 22 | 23 | 26 | 26 |
| -20 | 7 | 23 | 22 | 23 | 23 | 24 | 25 | 26 | 28 |

**Table 4-1** Number of Significant Bits in the Velocity Register

### *Velocity Register Resolution Equation*

The useful resolution of the Velocity Register data is calculated using the equation below, where n equals the number of significant bits from the previous table. Table 4-2 summarizes the useful velocity resolution for all gain combinations in µm/sec.

$$\text{Velocity Resolution} = 0.0029467 \times 2^{32-n} \quad \mu\text{m/sec}$$

| | Kp | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 |
|---|---|---|---|---|---|---|---|---|---|
| Kv | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| -6 | 0 | 96.55747 | X | X | X | X | X | X | X |
| -8 | 1 | 24.13937 | 48.27873 | 48.27873 | X | X | X | X | X |
| -10 | 2 | 6.03484 | 6.03484 | 12.06968 | 12.06968 | X | X | X | X |
| -12 | 3 | 96.55747 | 12.06968 | 1.50871 | 3.01742 | 3.01742 | X | X | X |
| -14 | 4 | 48.27873 | 48.27873 | 24.13937 | 12.06968 | 0.75436 | 1.50871 | X | X |
| -16 | 5 | 12.06968 | 24.13937 | 12.06968 | 12.06968 | 6.03484 | 0.37718 | 1.50871 | X |
| -18 | 6 | 3.01742 | 6.03484 | 6.03484 | 6.03484 | 3.01742 | 1.50871 | 0.18859 | 0.18859 |
| -20 | 7 | 1.50871 | 3.01742 | 1.50871 | 1.50871 | 0.75436 | 0.37718 | 0.18859 | 0.04715 |

**Table 4-2** Useful Velocity Register Resolution

# *Appendix A* VMEbus Register and Bit Assignments

The table that appears on the following pages is a summary of the offset address locations of the various registers on the ZMI-2002 Measurement Board. Also provided is the function for the each register bit. Use this table as a resource when programming the board for use in a VME backplane.

## Axis 1 Registers

| OFFSET | R/W | DESCRIPTION | BYTE 0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
| 1E | R | LSB Time | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 |
| 1C | R | MSB Time | T31 | T30 | T29 | T28 | T27 | T26 | T25 | T24 |
| 1E | W | EEPROM Data WR | EEDW15 | EEDW14 | EEDW13 | EEDW12 | EEDW11 | EEDW10 | EEDW9 | EEDW8 |
| 1C | W | EEPROM Control | | | | | | | PRE | PE |
| 1A | R | LSB Velocity | V15 | V14 | V13 | V12 | V11 | V10 | V9 | V8 |
| 18 | R | MSB Velocity | V31 | V30 | V29 | V28 | V27 | V26 | V25 | V24 |
| 1A | rW | P2 Interrupt Mask | | | | | | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 18 | rW | User Excess Velocity | EV15 | EV14 | EV13 | EV12 | EV11 | EV10 | EV9 | EV8 |
| 16 | R | LSB Sample Position | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 |
| 14 | R | MSB Sample Position | SP31 | SP30 | SP29 | SP28 | SP27 | SP26 | SP25 | SP24 |
| 16 | W | ADC Mux | | | | | | | | |
| 14 | rW | Data Age Adjust | | | | | | | | DA8 |
| 12 | R | LSB Position | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 |
| 10 | R | MSB Position | P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 |
| 12 | rW | LSB Offset | O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 |
| 10 | rW | MSB Offset | O31 | O30 | O29 | O28 | O27 | O26 | O25 | O24 |
| 0E M6 | R | Quick Reset High | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0E M5 | R | EEPROM Data RD | EEDR15 | EEDR14 | EEDR13 | EEDR12 | EEDR11 | EEDR10 | EEDR9 | EEDR8 |
| 0E M4 | R | Data Age Adjust | PMB8 | PMA8 | 0 | 0 | 0 | 0 | 0 | DA8 |
| 0E M3 | R | LSB Quick Reset | FR15 | FR14 | FR13 | FR12 | FR11 | FR10 | FR9 | FR8 |
| 0E M2 | R | LSB Offset | O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 |
| 0E M1 | R | User Excess Velocity | EV15 | EV14 | EV13 | EV12 | EV11 | EV10 | EV9 | EV8 |
| 0E M0 | R | High Nibbles | O35 | O34 | O33 | O32 | 0 | 0 | 0 | 0 |
| 0E | rW | High Nibbles | O35 | O34 | O33 | O32 | | | | |
| 0C M5 | R | P2 Interrupt Mask | 0 | 0 | 0 | 0 | 0 | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 0C M4 | R | Phase Meter Diag | PMB7 | PMB6 | PMB5 | PMB4 | PMB3 | PMB2 | PMB1 | PMB0 |
| 0C M3 | R | MSB Quick Reset | FR31 | FR30 | FR29 | FR28 | FR27 | FR26 | FR25 | FR24 |
| 0C M2 | R | MSB Offset | O31 | O30 | O29 | O28 | O27 | O26 | O25 | O24 |
| 0C M1 | R | Sample Timer | CNT15 | CNT14 | CNT13 | CNT12 | CNT11 | CNT10 | CNT9 | CNT8 |
| 0C M0 | R | Optical Power | 0 | 0 | 0 | 0 | 0 | 0 | OP9 | OP8 |
| 0C | rW | Sample Timer | CNT15 | CNT14 | CNT13 | CNT12 | CNT11 | CNT10 | CNT9 | CNT8 |
| 0A | RW | Control Register 2 | Disable Excess Velocity | Pos Direction Sense | Test | Enable 32 bit Overflow (ASIC revB) | Trigger Delay Enab | Reset Time RT2 | Reset Time RT1 | Reset Time RT0 |
| 08 | RW | Control Register 1 | VME Bit Window Enable | Bit Window A2 | Bit Window A1 | Bit Window A0 | P2 SCLK0 Output Enable | P2 SCLK0 Clock Disable | P2 D16 Select | P2 Latch Mode |
| 06 | RW | Interrupt Vector | Test | Interrupt Level 2 | Interrupt Level 1 | Interrupt Level 0 | | Readback MUX M2 | Readback MUX M1 | Readback MUX M0 |
| 04 | R | Error Status | IRQ Pending | | | | P2 External Sample | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 02 | RW | Interrupt Enable Register | Interrupt Inhibit | | | | P2 External Sample | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 00 | R | Status Register | 0 ASIC revA 1 ASIC revB | 0 | 0 | 0 | 0 | 0 | 0 | External Sample Flag |
| 00 | W | Command Register | | | | | Reset P2 Ext Sample Interrupt | Reset 32 bit Position Overflow | Sample VME Position | External Sample (SCLK0) |

Notes: rW indicates Write with Read accessed through a different address, RW indicates Write with Readback, Test indicates factory test.

## Axis 1 Registers

| OFFSET | BYTE 1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 1E | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| 1C | T23 | T22 | T21 | T20 | T19 | T18 | T17 | T16 |
| 1E | EEDW7 | EEDW6 | EEDW5 | EEDW4 | EEDW3 | EEDW2 | EEDW1 | EEDW0 |
| 1C | EEOP1 | EEOP0 | EEA5 | EEA4 | EEA3 | EEA2 | EEA1 | EEA0 |
| 1A | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |
| 18 | V23 | V22 | V21 | V20 | V19 | V18 | V17 | V16 |
| 1A | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 18 | EV7 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |
| 16 | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |
| 14 | SP23 | SP22 | SP21 | SP20 | SP19 | SP18 | SP17 | SP16 |
| 16 | | | | | AM3 | AM2 | AM1 | AM0 |
| 14 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| 12 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| 10 | P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 |
| 12 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
| 10 | O23 | O22 | O21 | O20 | O19 | O18 | O17 | O16 |
| 0E M6 | 0 | FR38 | FR37 | FR36 | FR35 | FR34 | FR33 | FR32 |
| 0E M5 | EEDR7 | EEDR6 | EEDR5 | EEDR4 | EEDR3 | EEDR2 | EEDR1 | EEDR0 |
| 0E M4 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| 0E M3 | FR7 | FR6 | FR5 | FR4 | FR3 | FR2 | FR1 | FR0 |
| 0E M2 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
| 0E M1 | EV7 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |
| 0E M0 | SP35 | SP34 | SP33 | SP32 | P35 | P34 | P33 | P32 |
| 0E | | | | | | | | |
| 0C M5 | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 0C M4 | PMA7 | PMA6 | PMA5 | PMA4 | PMA3 | PMA2 | PMA1 | PMA0 |
| 0C M3 | FR23 | FR22 | FR21 | FR20 | FR19 | FR18 | FR17 | FR16 |
| 0C M2 | O23 | O22 | O21 | O20 | O19 | O18 | O17 | O16 |
| 0C M1 | CNT7 | CNT6 | CNT5 | CNT4 | CNT3 | CNT2 | CNT1 | CNT0 |
| 0C M0 | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| 0C | CNT7 | CNT6 | CNT5 | CNT4 | CNT3 | CNT2 | CNT1 | CNT0 |
| 0A | Test | KP2 | KP1 | KP0 | Test | KV2 | KV1 | KV0 |
| 08 | Reserved | P2 RESET Time Reset Enable | P2 RESET Quick Reset Enable | P2 RESET Reset Position Enable | P2 RESET Error Reset Enable | Test | User P2 | User LED |
| 06 | IV7 | IV6 | IV5 | IV4 | IV3 | IV2 | IV1 | IV0 |
| 04 | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 02 | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 00 | EEPROM Busy | ADC Mux=0 | ADC Ready | Position Reset Complete | Measure Present Status | Reference DLL Status | Reference PLL Status | Reference Present Status |
| 00 | Reset User Velocity Error | Reset Time | Reset Position Quick | Reset Position | | | | Reset Axis |

## Axis 2 Registers

| OFFSET | R/W | DESCRIPTION | BYTE 0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
| 3E | R | LSB Time | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 |
| 3C | R | MSB Time | T31 | T30 | T29 | T28 | T27 | T26 | T25 | T24 |
| 3E | W | Reserved | | | | | | | | |
| 3C | W | Reserved | | | | | | | | |
| 3A | R | LSB Velocity | V15 | V14 | V13 | V12 | V11 | V10 | V9 | V8 |
| 38 | R | MSB Velocity | V31 | V30 | V29 | V28 | V27 | V26 | V25 | V24 |
| 3A | rW | P2 Interrupt Mask | | | | | | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 38 | rW | User Excess Velocity | EV15 | EV14 | EV13 | EV12 | EV11 | EV10 | EV9 | EV8 |
| 36 | R | LSB Sample Position | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 |
| 34 | R | MSB Sample Position | SP31 | SP30 | SP29 | SP28 | SP27 | SP26 | SP25 | SP24 |
| 36 | W | Reserved | | | | | | | | |
| 34 | rW | Data Age Adjust | | | | | | | | DA8 |
| 32 | R | LSB Position | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 |
| 30 | R | MSB Position | P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 |
| 32 | rW | LSB Offset | O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 |
| 30 | rW | MSB Offset | O31 | O30 | O29 | O28 | O27 | O26 | O25 | O24 |
| 2E M6 | R | Quick Reset High | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2E M5 | R | Reserved | | | | | | | | |
| 2E M4 | R | Data Age Adjust | PMB8 | PMA8 | 0 | 0 | 0 | 0 | 0 | DA8 |
| 2E M3 | R | LSB Quick Reset | FR15 | FR14 | FR13 | FR12 | FR11 | FR10 | FR9 | FR8 |
| 2E M2 | R | LSB Offset | O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 |
| 2E M1 | R | User Excess Velocity | EV15 | EV14 | EV13 | EV12 | EV11 | EV10 | EV9 | EV8 |
| 2E M0 | R | High Nibbles | O35 | O34 | O33 | O32 | 0 | 0 | 0 | 0 |
| 2E | rW | High Nibbles | O35 | O34 | O33 | O32 | | | | |
| 2C M5 | R | P2 Interrupt Mask | 0 | 0 | 0 | 0 | 0 | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 2C M4 | R | Phase Meter Diag | PMB7 | PMB6 | PMB5 | PMB4 | PMB3 | PMB2 | PMB1 | PMB0 |
| 2C M3 | R | MSB Quick Reset | FR31 | FR30 | FR29 | FR28 | FR27 | FR26 | FR25 | FR24 |
| 2C M2 | R | MSB Offset | O31 | O30 | O29 | O28 | O27 | O26 | O25 | O24 |
| 2C M1 | R | Reserved | | | | | | | | |
| 2C M0 | R | Reserved | | | | | | | | |
| 2C | rW | Reserved | | | | | | | | |
| 2A | RW | Control Register 2 | Disable Excess Velocity | Pos Direction Sense | Test | Enable 32 bit Overflow (ASIC revB) | Trigger Delay Enab | Reset Time RT2 | Reset Time RT1 | Reset Time RT0 |
| 28 | RW | Control Register 1 | VME Bit Window Enable | Bit Window A2 | Bit Window A1 | Bit Window A0 | | | P2 D16 Select | P2 Latch Mode |
| 26 | RW | Interrupt Vector | Test | Interrupt Level 2 | Interrupt Level 1 | Interrupt Level 0 | | Readback MUX M2 | Readback MUX M1 | Readback MUX M0 |
| 24 | R | Error Status | IRQ Pending | | | | P2 External Sample | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 22 | RW | Interrupt Enable Register | Interrupt Inhibit | | | | P2 External Sample | 32 bit Position Overflow | 36 bit Position Overflow | Acceleration Error |
| 20 | R | Status Register | 0 ASIC revA 1 ASIC revB | 0 | 0 | 0 | 0 | 0 | 0 | External Sample Flag |
| 20 | W | Command Register | | | | | Reset P2 Ext Sample Interrupt | Reset 32 bit Position Overflow | Sample VME Position | |

Notes: rW indicates Write with Read accessed through a different address, RW indicates Write with Readback, Test indicates factory test.

## Axis 2 Registers

| OFFSET | BYTE 1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 3E | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| 3C | T23 | T22 | T21 | T20 | T19 | T18 | T17 | T16 |
| 3E | | | | | | | | |
| 3C | | | | | | | | |
| 3A | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |
| 38 | V23 | V22 | V21 | V20 | V19 | V18 | V17 | V16 |
| 3A | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 38 | EV7 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |
| 36 | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |
| 34 | SP23 | SP22 | SP21 | SP20 | SP19 | SP18 | SP17 | SP16 |
| 36 | | | | | | | | |
| 34 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| 32 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| 30 | P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 |
| 32 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
| 30 | O23 | O22 | O21 | O20 | O19 | O18 | O17 | O16 |
| 2E M6 | 0 | FR38 | FR37 | FR36 | FR35 | FR34 | FR33 | FR32 |
| 2E M5 | | | | | | | | |
| 2E M4 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| 2E M3 | FR7 | FR6 | FR5 | FR4 | FR3 | FR2 | FR1 | FR0 |
| 2E M2 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
| 2E M1 | EV7 | EV6 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |
| 2E M0 | SP35 | SP34 | SP33 | SP32 | P35 | P34 | P33 | P32 |
| 2E | | | | | | | | |
| 2C M5 | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 2C M4 | PMA7 | PMA6 | PMA5 | PMA4 | PMA3 | PMA2 | PMA1 | PMA0 |
| 2C M3 | FR23 | FR22 | FR21 | FR20 | FR19 | FR18 | FR17 | FR16 |
| 2C M2 | O23 | O22 | O21 | O20 | O19 | O18 | O17 | O16 |
| 2C M1 | | | | | | | | |
| 2C M0 | | | | | | | | |
| 2C | | | | | | | | |
| 2A | Test | KP2 | KP1 | KP0 | Test | KV2 | KV1 | KV0 |
| 28 | Reserved | P2 RESET Time Reset Enable | P2 RESET Quick Reset Enable | P2 RESET Reset Position Enable | P2 RESET Error Reset Enable | Test | User P2 | |
| 26 | IV7 | IV6 | IV5 | IV4 | IV3 | IV2 | IV1 | IV0 |
| 24 | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 22 | User Velocity Error | Velocity Error | Measure Signal Glitch | Measure Signal Dropout | Measure Signal Missing | Reference DLL Error | Reference PLL Error | Reference Signal Missing |
| 20 | EEPROM Busy | ADC Mux=0 | ADC Ready | Position Reset Complete | Measure Present Status | Reference DLL Status | Reference PLL Status | Reference Present Status |
| 20 | Reset User Velocity Error | Reset Time | Reset Position Quick | Reset Position | | | | Reset Axis |

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